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1. ABSTRACT

THIS PROGRAM IS A MEMORY EXPANDABLE INTERACTIVE BUS EXERCISER FOR A PAPER TAPE ORIENTED PDP-11/20. IT PERFORMS A TEST OF INSTRUCTIONS AND CONCURRENT OPERATIONS OF I/O EQUIPMENT SIMULTANEOUSLY. IT MAY ALSO PERFORM THE SAME OPERATION INDEPENDENTLY. THIS PROGRAM IS NOT TO BE CONSIDERED A TOTAL CHECK OF THE SYSTEM. IF AN ERROR IS DETECTED IN AN I/O DEVICE, IT WILL PROBABLY BE NECESSARY TO CORRECT THE MALFUNCTION WITH THE RESPECTIVE DIAGNOSTIC FOR THAT DEVICE.

IN THIS VERSION THE INTERRUPT SERVICE ROUTINE FOR THE DISKS, KW11L, PLUS THE STACK AND THE NRP DATA BUFFERS ARE RELOCATED TO THE CURRENT BANK.

2. REQUIREMENTS

2.1 EQUIPMENT

PDP-11/20 STANDARD COMPUTER

2.1.1 OPTIONAL HARDWARE THAT THE PROGRAM WILL EXERCISE

MM11	UP TO 28KW OF MEMORY
RC11	DISK
RK11	DISK
RP11	DISK
RF11	DISK (256K)
TC11	DECTAPE-TRANSPORT ZERO
KE11	EXTENDED ARITHMETIC UNIT
KW11L	LINE CLOCK
PC11	HIGH SPEED READER/PUNCH
KL11	ASR33 OR ASR35 TELEPRINTER-LC11, VT05
LP11	LINE PRINTER

2.2 STORAGE

2.2.1 PROGRAM STORAGE -- THE ROUTINE USES MEMORY FROM 0000 TO 17476.

3. LOADING PROCEDURE

3.1 METHOD

PROCEDURE FOR NORMAL ABSOLUTE TAPES SHOULD BE FOLLOWED.

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4. STARTING PROCEDURE

4.1 CONTROL SWITCH SETTING

STARTING AT SA 200 ALL SWITCHES SHOULD BE SET AS INDICATED.

4.2 STARTING ADDRESS OR ADDRESSES

- (A) 200 = SR = 000777 TEST PROCESSOR ONLY=WITH CORE EXPANSION
- (B) 200 = SR = 001777 TEST PROCESSOR ONLY=4K-INHIBIT
CORE EXPANSION
- (C) 200 = SF = 002XXX TEST I/O ONLY
- (D) 200 = SR = 000000 -CORE EXPAND AND TEST ALL AVAILABLE
I/O DEVICES

SW0 = 1 INHIBIT TTY OUTPUT
SW1 = 1 INHIBIT TTY INPUT
SW2 = 1 INHIBIT HSP
SW3 = 1 INHIBIT HSR
SW4 = 1 INHIBIT LINE CLOCK
SW5 = 1 INHIBIT RF11, RK11, RC11 AND RP11 DISK(S)
SW6 = 1 INHIBIT TC11 DECTAPE
SW7 = 1 INHIBIT LINE PRINTER --- IF LINE PRINTER IS USED.
MUST RESTART AT 400
IF EAE EXIST IT WILL BE AUTOMATICALLY SELECTED

4.3 PROGRAM AND/OR OPERATOR ACTION

LOAD PROGRAM INTO MEMORY,
SET SWITCH REGISTER TO STARTING ADDRESS,
LOAD ADDRESS.
SET SWITCHES TO INHIBIT NON EXISTANT DEVICES
PRESS START.
THE PROGRAM WILL LOOP AND
BELL WILL RING ONCE PER PASS OF THE PROGRAM,
A MINIMUM OF TWO PASSES SHOULD
ALWAYS BE RUN.

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5. OPERATING PROCEDURE

5.1 OPERATIONAL SWITCH SETTINGS

5.1.1 AT SA 200 ., THE INSTRUCTION AND LOGIC TEST, WITH ALL SWITCHES DOWN THE PROGRAM WILL TEST ALL DEVICES AND PRINT OUT ON ERRORS AND CONTINUE IN TEST. (BELL WILL RING AT COMPLETION OF A PASS)

5.1.2 SWITCH SETTINGS ARE

SW15 = 1 OR UP ... HALT ON ERROR
SW14 = 1 OR UP ... SCOPE LOOP
SW13 = 1 OR UP ... INHIBIT PRINTOUT
SW12 = 1 OR UP ... INHIBIT TRACE TRAPPING
SW11 = 1 OR UP ... INHIBIT ITERATION LOOP
SW10 = 1 OR UP ... INHIBIT PROCESSOR TEST
SW09 = 1 OR UP ... INHIBIT VARIABLE CORE EXPANSION
SW08 = 1 OR UP ... RESTART ON ERROR

5.1.3

5.2. SUBROUTINE ABSTRACTS

5.2.1 BEGIN SA 200

5.2.2 SCOPE

THIS SUBROUTINE CALL IS PLACED BETWEEN EACH SUBTEST IN THE INSTRUCTION SECTION. IT RECORDS THE STARTING ADDRESS OF EACH SUB-TEST AS IT IS BEING ENTERED. IF A SCOPE LOOP IS REQUESTED, IT WILL JUMP TO THE START OF THE SUBTEST THAT THE SCOPE LOOP IS REQUESTED FOR. IF SCOPE LOOP IS NOT REQUESTED, THERE WILL BE EITHER A FIXED OR RANDOM NUMBER OF ITERATIONS ON THAT SUB-TEST BEFORE THE NEXT SUBTEST IS ENTERED. SWITCH 11 ON A 1 INHIBITS ITERATION OF SUBTESTS.

5.2.3 HLT

IS A ROUTINE THAT PRINTS-OUT AN ADDRESS THAT TAGS THE FAILING SUBTEST, AND THE STATUS REGISTER AT THE TIME OF THE FAILURE.

5.2.4 TRTRAP

THIS ROUTINE WILL ALLOW THE TRACE BIT TRAP TO BE SET AFTER FIRST LOOP OF THE PROGRAM. UNDER NORMAL TESTING THE TRACE BIT WILL BE SET ON ALTERNATE LOOPS OF THE PROGRAM. WHEN SET IT CAUSES A TRAP AFTER EACH INSTRUCTION. THE FIRST INSTRUCTION EXECUTED UPON TRAPPING IS AN "RTI" WHICH RETURNS TO THE INTERRUPTED SEQUENCE OF INSTRUCTION. THIS SEQUENCE IS CONTINUED TILL THE END OF THE PROGRAM LOOP IS REACHED.

(5. OPERATING PROCEDURE CONT'D)

5.2.5 TRAPCATCHER

THIS IS A SERIES OF INSTRUCTIONS STARTING AT LOCATION Z, DESIGNED TO DETECT, AND ISOLATE UNEXPECTED TRAPS AND INTERRUPTS TO THE TRAP AND INTERRUPT VECTOR AREA OF MEMORY.

THE PRINCIPAL OF THIS ROUTINE IS: THE VECTOR ENTRANCE ADDRESS POINTS TO THE NEXT SEQUENTIAL WORD WHICH CONTAINS A HALT (00000), (THIS LOCATION IS ALSO THE STATUS FOR THAT VECTOR ENTRANCE, BUT THIS HAS NO EFFECT ON IT ALSO BEING THE NEXT INSTRUCTION).

IF A HALT OCCURS IN THE TRAP OR INTERRUPT VECTOR AREA, REGISTER SIX SHOULD BE EXAMINED TO DETERMINE ITS CONTENTS, THEN USE REGISTER SIX CONTENTS AS AN ADDRESS TO DETERMINE THE LOCATION WHERE THE PROGRAM WAS AT, WHEN THE INTERRUPT OR TRAP OCCURRED, (MEMORY AS SPECIFIED BY R6 CONTAINS THE PC OF THE INSTRUCTION FOLLOWING THE INSTRUCTION WHERE THE TRAP OCCURRED).

5.2.6 TTYIN1 (TTY INPUT)

THIS ROUTINE OPERATES IN THE INTERRUPT MODE AND CHECKS FOR A COUNT PATTERN IN THE READER OF THE TTY. THE ROUTINE WILL ACCEPT AN INFINITE NUMBER OF ZERO BYTES (BLANK TAPE). BUT THE FIRST BYTE THAT IS NOT A ZERO MUST BE A ONE AND ALL SEQUENTIAL BYTES MUST BE ONE GREATER. IF THE ROUTINE DETECTS AN ERROR IN THE COUNT PATTERN, IT CHECKS TO SEE IF IT IS A 207 (BELL). IF SO IT IS IGNORED, IF NOT A COMPARISON ERROR IS FLAGGED.

5.2.7 TTYOUT (TTY OUTPUT)

THIS IS A ROUTINE THAT OUTPUTS A COUNT PATTERN IN THE INTERRUPT MODE TO THE TELEPRINTER. IF A PAPER TAPE IS PUNCHED IT MAY HAVE 207'S (BELLS) IN IT, PUNCHED WHEN THE BELL FOR PASS COMPLETE RINGS.

5.2.8 PFSTART (RF-11 DISK)

THIS ROUTINE PERFORMS A WRITE AND A WRITE CHECK OF THE DISK. THE DATA THAT IS WRITTEN ON THE DISK IS PART OF TEST PROGRAM CODE THAT IS NEVER MODIFIED. THIS SEGMENT OF CORE IS WRITTEN IN CONTIGUOUS BLOCK THRU THE DISK MEMORY. AFTER THE TOTAL DISK(S) HAS BEEN WRITTEN, A WRITE CHECK IS USED TO VERIFY THAT THE DATA HAS BEEN WRITTEN CORRECTLY ON THE DISK. NOTE THAT NO

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"DAT!" ARE USED IN EXERCISING THE DISK (DATA IS NOT TRANSFERRED INTO CORE). THERE IS A LOCATION IN THE PROGRAM THAT IF MODIFIED WILL ALLOW EXERCISING UP TO EIGHT DISKS. THE INTERRUPT SERVICE ROUTINE AND DATA BUFFER IS TRANSFERRED TO THE CURRENT BANK THAT INSTRUCTIONS ARE BEING EXECUTED IN.

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5.2.9 FENDZ (TC11 FORWARD END ZONE)

FENDZ IS THE FIRST ADDRESS IN THE DECTAPE INTERRUPT VECTOR (214). THIS ROUTINE WILL READ, IN REVERSE, BLOCK NUMBERS UNTIL THE REVERSE END ZONE IS FOUND. AT THIS POINT THE INTERRUPT VECTOR AND COMMAND REGISTER ARE MODIFIED TO READ ALL BLOCK NUMBERS IN THE FORWARD DIRECTION. EACH BLOCK NUMBER READ IS COMPARED WITH THE EXPECTED BLOCK NUMBER COUNT AND MISCOMPARISONS REPORTED. WHEN EACH BLOCK IS FOUND (WITH THE EXCEPTION OF BLOCK 0) A BLOCK (400 WORDS) OF TEST DATA IS WRITTEN ONTO TAPE. AFTER ALL BLOCK NUMBERS HAVE BEEN READ THE TAPE IS DRIVEN INTO THE FORWARD END ZONE, HERE THE DIRECTION IS REVERSED AND ALL BLOCK NUMBERS ARE READ IN REVERSE. STARTING WITH BLOCK 1100 THROUGH BLOCK 1 THE DATA IS READ FROM TAPE. THE SAME BUFFER IS USED FOR BOTH READ AND WRITE OPERATIONS. THE DATA IN THE BUFFER IS CHECK-SUMMED DURING THE READ OPERATION. IF THE DATA-BUFFER IS DESTROYED DURING A READ OPERATION IT MAY BE NECESSARY TO RELOAD THE PROGRAM.

5.2.10 LCLK (LINE CLOCK)

THIS TEST OF THE LINE CLOCK IS IN THE INTERRUPT MODE. IF OPERATING CORRECTLY THE SYSTEM I/O WILL RUN A FULL SPEED FOR 55 SECONDS THEN ALL I/O AT LEVEL FOUR OR LESS WILL STALL FOR 5 SECONDS. THIS IS BASED ON 60 CYCLES AS THE LINE FREQUENCY.

5.2.11 LP1 (LINE PRINTER)

THIS ROUTINE OUTPUTS TO THE LINE PRINTER IN THE FLAG MODE WHILE FILLING THE BUFFER IN THE INTERRUPT MODE WHILE THE BUFFER IS BEING PRINTED.

5.2.12 HSRIM1 (PC11 INPUT)

THIS ROUTINE OPERATES IN THE INTERRUPT MODE AND CHECKS FOR A COUNT PATTERN IN THE PC11 READER. THE ROUTINE WILL ACCEPT AN INFINITE NUMBER OF ZERO BYTES (BLANK TAPE). BUT THE FIRST BYTE THAT IS NOT A ZERO MUST BE A ONE AND ALL SEQUENTIAL BYTES MUST BE ONE GREATER. IF THE ROUTINE DETECTS AN ERROR IN THE COUNT PATTERN, A DATA ERROR IS FLAGGED.

5.2.13 HPOUT (PC11 OUTPUT)

THIS IS A ROUTINE THAT OUTPUTS A COUNT PATTERN IN THE INTERRUPT MODE TO THE HIGH SPEED PUNCH.

5.2.14 RKSTART (RK=11 DISK)

THIS ROUTINE PERFORMS A WRITE AND A WRITE CHECK OF THE DISK. THE DATA THAT IS WRITTEN ON THE DISK IS PART OF TEST PROGRAM CODE THAT IS NEVER MODIFIED. THIS SEGMENT OF CORE IS WRITTEN IN CONTIGUOUS BLOCK THRU THE DISK MEMORY. AFTER THE TOTAL DISK HAS BEEN WRITTEN, A WRITE CHECK IS USED TO VERIFY THAT THE DATA HAS BEEN WRITTEN CORRECTLY ON THE DISK. NOTE THAT NO "DATI" ARE USED IN EXERCISING THE DISK (DATA IS NOT TRANSFERRED INTO CORE). THE INTERRUPT SERVICE ROUTINE AND DATA BUFFER ARE TRANSFERRED TO THE CURRENT BANK THAT INSTRUCTIONS ARE BEING EXECUTED IN.

5.2.15 RESTART (RE=11 DISK)

THIS ROUTINE PERFORMS A WRITE AND A WRITE CHECK OF THE DISK. THE DATA THAT IS WRITTEN ON THE DISK IS PART OF TEST PROGRAM CODE THAT IS NEVER MODIFIED. THIS SEGMENT OF CORE IS WRITTEN IN CONTIGUOUS BLOCK THRU THE DISK MEMORY. AFTER THE TOTAL DISK(S) HAS BEEN WRITTEN, A WRITE CHECK IS USED TO VERIFY THAT THE DATA HAS BEEN WRITTEN CORRECTLY ON THE DISK. NOTE THAT NO "DATI" ARE USED IN EXERCISING THE DISK (DATA IS NOT TRANSFERRED INTO CORE). THERE IS A LOCATION IN THE PROGRAM THAT IF MODIFIED WILL ALLOW EXERCISING UP TO FOUR DISKS. THE INTERRUPT SERVICE ROUTINE AND DATA BUFFER IS TRANSFERRED TO THE CURRENT BANK THAT INSTRUCTIONS ARE BEING EXECUTED IN.

5.2.16 RPSTART (RP=11 DISK)

THIS ROUTINE PERFORMS A WRITE AND A WRITE CHECK OF THE DISK. THE DATA THAT IS WRITTEN ON THE DISK IS PART OF TEST PROGRAM CODE THAT IS NEVER MODIFIED. THIS SEGMENT OF CORE IS WRITTEN IN CONTIGUOUS BLOCK THRU THE DISK MEMORY. AFTER THE TOTAL DISK(S) HAS BEEN WRITTEN, A WRITE CHECK IS USED TO VERIFY THAT THE DATA HAS BEEN WRITTEN CORRECTLY ON THE DISK. NOTE THAT NO "DATI" ARE USED IN EXERCISING THE DISK (DATA IS NOT TRANSFERRED INTO CORE). THE INTERRUPT SERVICE ROUTINE AND DATA BUFFER IS TRANSFERRED TO THE CURRENT BANK THAT INSTRUCTIONS ARE BEING EXECUTED IN.

5.2.17 CORE EXPANSION (DET1)

THIS ROUTINE IS CONTROLLED BY SWITCH 9. THE PROCESSOR MAINLINE CODE WILL BE EITHER 4KW OR EXPANDS TO THE MAXIMUM CORE THAT IS AVAILABLE. THE ROUTINE DETERMINES THE MAXIMUM CORE SIZE BY DOING A "DATO" TO A LOCATION IN EACH BANK. IF THE BANK DOES NOT EXIST, A TIME OUT WILL OCCUR. WHEN CORE SIZE IS DETERMINED AN IMAGE OF BANK 0 IS TRANSFERRED TO EACH EXISTING BANK. THEN THE CODE IN EACH BANK IS MODIFIED SO THAT, WHEN THE LAST SUB TEST IN A MEMORY BANK IS EXECUTED THERE IS A JUMP INSERTED TO THE FIRST SUB TEST OF THE NEXT BANK. WHEN IN THE LAST BANK THE MODIFIED INSTRUCTION WILL TRANSFER YOU TO BANK 0.

THE LISTING SHOWS ONLY THE CODE OF BANK ZERO. WHEN AN ERROR OCCURS THAT IS NOT IN BANK ZERO, IGNORE THE BANK BITS OF THE PRINT OUT AND USE THE LISTING FOR BANK ZERO.

5.3 PROGRAM AND/OR OPERATOR ACTION

- 5.3.1 LOADING AND STARTING AT 200 WITH ALL SWITCHES DOWN IS WORSE CASE TESTING. IF AN ERROR IS DETECTED HERE, THERE WILL BE A PRINTOUT. WHEN AN ERROR IS DETECTED AND IT IS NECESSARY TO SCOPE ON IT, PLACE SW15 UP TO HALT ON ERROR, THEN SW14 UP TO LOOP ON ERROR, THEN SW13 UP TO DELETE PRINTOUTS. WHEN TESTING THE HSR OR TTY READER THE TAPE MUST HAVE A COUNT PATTERN AND BE LOCATED ON THE LEADER PORTION WHEN STARTING TEST.

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6. ERRORS.

6.1 ERROR PRINTOUT

ARE IN A TWO WORD FORMAT, THE 1ST IS PC+2 OF THE
DETECED ERROR, THE 2ND, IS THE STATUS REGISTER.
REFER TO THE LISTING FOR DETAILED INFORMATION.

6.2 ERROR RECOVERY

FOR TTY READER AND HSR, TAPE MUST BE REPOSITIONED TO
LEADER BEFORE RESTARTING TEST.

7. RESTRICTIONS

7.1 STARTING RESTRICTION

IF LINE PRINTER IS USED RESTART ADDRESS MUST BE 400
FOR HSR AND TTY READER, TAPE MUST BE ON LEADER.

7.2 OPERATIONAL RESTRICTION

NONE

8. MISCELLANEOUS

TRACKING DOWN UNUSUAL FAILURES

FAILURES THAT MAY OCCUR BECAUSE OF A FALSE ENTRY INTO A SUBTEST, OR A FAILURE IN A CONTROL ROUTINE RATHER THAN A SUBTEST. DETECTION OF THESE MAY BE ACCOMPLISHED BY SEVERAL PROCEDURES. THERE IS A LOCATION CALLED "RETURN" THAT RECORDS THE LAST SUCCESSFUL SUBTEST COMPLETED. THERE IS ANOTHER LOCATION CALLED "SCOPEF" THAT SHOWS HOW MANY TIMES THE SUBTEST HAS BEEN EXECUTED. THERE IS ANOTHER LOCATION CALLED "ICOUNT" THAT CONTAINS THE ITERATION COMPARISON VALUE. THE STACK "R6" SHOULD BE EQUAL TO "RUFF" WHEN THE FIRST INSTRUCTION OF THE SUBTEST IS ENTERED. TO REDUCE INSTRUCTION EXECUTION IN CONFUSING SITUATION, THE "SCOPE" LOCATION FOLLOWING THE SUBTEST SHOULD BE CHANGED TO A BRANCH TO THE FIRST INSTRUCTION OF THE SUBTEST (THE FIRST LOCATION FOLLOWING THE PREVIOUS SCOPE LOCATION) AND THE "HLT" LOCATION MAY BE REPLACED WITH A "NOP".

A USER MAY ADD A UNIQUE ROUTINE TO THIS TEST TO EXERCISE A NON DEC OPTION, FOR CHECKING BUS INTERACTION WITH HIS EXISTING DEC OPTIONS.

FOR TROUBLE FREE INTERACTION THERE ARE A FEW GROUND RULES THAT SHOULD BE FOLLOWED.

1. USE NO REGISTERS.
2. THE ROUTINE SHOULD BE STAND ALONE.
3. THE EXISTING "HLT" SHOULD BE USED FOR ERROR DETECTION.
4. CODE IN THE PRIMING AREA SHOULD SET INTERRUPT ENABLE, INITIALIZE DATA AND RAISE A FLAG IF NECESSARY.
5. THE INTERRUPT VECTOR STATUS WORD SHOULD CONTAIN THE PRIORITY LEVEL OF THE DEVICE.
6. THE INTERRUPT VECTOR SHOULD POINT TO YOUR STAND ALONE ROUTINE.
7. THE STAND ALONE ROUTINE WHEN COMPLETING ALL HOUSE KEEPING OPERATION AND DATA COMPARISONS SHOULD THEN EXECUTE A "RTI" TO RETURN TO MAINLINE CODE.

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(B. CONT'D)

INSERTION OF USER I/O ROUTINES

1. MAY BE INSERTED IN BANK ZERO WHERE I/O ROUTINES EXIST. FOR DEVICES THAT THE USER DOES NOT HAVE, IF CORE EXPANSION IS TO BE INHIBITED, THE USER MAY OVERLAY THE EXPANSION CODE.
2. IF THE USER HAS MORE THAN 4KW OF CORE, THE ROUTINE MAY BE PLACED IN ANY OF THE EXTRA BANKS AND CORE EXPANSION BE INHIBITED.
3. IN THE PRIMING CODE SEVERAL INSTRUCTIONS BEFORE THE TAG "MAINLINE" THERE IS AN INSTRUCTION JSR %7,@#USER. THE SECOND WORD OF THAT INSTRUCTION IS AN ABSOLUTE ADDRESS THAT THE USER MAY CHANGE TO POINT TO HIS ROUTINE. THE USER SHOULD EXIT HIS PRIMING ROUTINE WITH A RTS %7 INSTRUCTION.

8.1 EXECUTION TIME

EXECUTION VARIES WITH NUMBER OF DEVICES, FOR 4KW SYSTEMS WITH TTY AND HSR ONLY, ABOUT 1 MINUTE WITH THE TRACE BIT CLEARED ABOUT 1.5 MINUTES WITH THE TRACE BIT SET.

WITH 28KW SYSTEMS USING TTY AND HSR WITH TRACE BIT CLEARED AND WITH TRACE BIT SET.

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9, PROGRAM DESCRIPTION

THE DESIGN OF THIS SYSTEM EXERCISER IS PREDICATED UPON IT BEING PRIMARILY INTENDED FOR A PAPER TAPE SYSTEM WITH FOUR KW OF CORE, AND THAT IT BE EASY TO RUN AND UNDERSTAND. ALSO, THAT IT MAY BE MODIFIED EASILY TO EXERCISE A WIDE MULTITUDE OF PERIPHERALS, INCLUDING THOSE OF THE CUSTOMER'S OWN DESIGN. THE CONCEPT IS TO HAVE ALL DESIRED I/O RUNNING CONCURRENTLY WITH THE PROCESSOR TEST FOR BACKGROUND. THE DECISION WHICH I/O DEVICES TO BE USED IS MADE AT START UP TIME. THE DATA PATTERNS USED IN THE EXERCISER ARE FIXED. FOR MECHANICAL DEVICES, SUCH AS THE TTY READER, THERE IS NO AUTOMATIC RE-SYNCHRONIZATION IF IT'S TAPE BECOMES OUT OF PHASE WITH THE DATA. IT WILL BECOME NECESSARY TO STOP THE EXERCISEP AND MANUALLY RESYNCHRONIZE THE TAPE AND RESTART THE EXERCISER.

THERE IS NO MONITOR IN THE CONVENTIONAL SENSE. EACH DEVICE THAT IS TO BE EXERCISED HAS IT'S OWN STAND ALONE ROUTINE THAT OPERATES IN THE INTERRUPT MODE, THESE ROUTINES NEED NO SUPERVISION OR MONITORING AFTER THEY ARE INITIATED. THERE IS A PRIMER AREA THAT CHECKS THE SWITCH REGISTER TO SEE WHAT DEVICES ARE TO BE INITIATED. THE PRIMER AREA SETS THE INTERRUPT ENABLE BIT IN THE DEVICE STATUS REGISTER, INITIALIZES THE DATA PATTERN AND INITIATES AN OPERATION TO RAISE DATA FLAGS ON DEVICES THAT CAN NOT INITIATE THEM THEMSELVES. THEN, THE PRIMER JUMPS TO THE PROCESSOR TEST WHERE THE INDIVIDUAL DEVICES ARE SERVICED AT THE INTERRUPT RATE.

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9. PROGRAM DESCRIPTION - CONTINUED

THE INSTRUCTION EXERCISER IS A STRAIGHT LINE TEST OF INSTRUCTIONS. THE SEQUENCE IN WHICH THEY ARE EXECUTED IS THE SAME SEQUENCE IN WHICH THEY ARE SHOWN IN THE LISTING. EACH AREA OF CODE FROM "SCOPE TO SCOPE" IS AN INDIVIDUAL SUB-TEST, WITH SWITCH 11 UP THE SUB-TEST IS EXECUTED ONE TIME AND THEN THE NEXT SUB-TEST IS EXECUTED, AND SO ON TILL ALL SUB-TESTS ARE EXECUTED. HOWEVER IF SWITCH 11 IS DOWN THE SUB-TEST WILL BE EXECUTED SOME "N" NUMBER OF TIMES BEFORE ENTERING THE NEXT SUB-TEST. IF SWITCH 14 IS UP YOU WILL NEVER LEAVE THE CURRENT SUB-TEST YOU ARE IN. THIS USE IS INTENDED FOR TROUBLE SHOOTING A MALFUNCTION IN A SUB-TEST. THE FIRST GROUP OF SUB-TESTS ARE THE BINARYS AND UNARYS. THOSE INSTRUCTIONS ARE TESTED IN THE INDEX MODE: SOURCE ONLY, DESTINATION ONLY, THEN BOTH SOURCE AND DESTINATION. THE SAME INSTRUCTIONS ARE THEN TESTED USING THE IMMEDIATE MODE INDIRECT. THESE MODES ARE TESTED AGAINST OTHER MODES; WHICH MAY USE A REGISTER OR MEMORY LOCATION. THESE WILL BE SWAPPED BETWEEN SOURCE AND DESTINATION.

AFTER THE MODES AND INSTRUCTION HAVE BEEN PROVEN IN THE WORD MODE, THEY ARE THEN TESTED IN THE BYTE MODE. OTHER TESTING IS ALSO DONE WHERE THE "JSR" INSTRUCTION IS TESTED IN NESTED COMBINATIONS. ALL COMBINATIONS OF NUMBERS ARE TESTED USING THE COMPARE, ROTATE, ADD AND COMPLIMENT INSTRUCTIONS. THERE IS ALSO A MINIMUM TEST OF POWER FAIL AND AUTO RECOVERY, WHICH IS NOT ENABLED UNTIL AFTER THE FIRST PASS OF THE PROGRAM. THE PROGRAM REQUIRES TWO BELLS ON THE TTY TO MAKE ONE TRUE PASS OF THE PROGRAM. THE FIRST BELL OCCURS AFTER ONE PASS OF THE INSTRUCTION TEST WITH THE TRACE BIT CLEARED. THE SECOND BELL MARKS THE END OF AN INSTRUCTION TEST PASS WITH THE TRACE BIT SET. THE REASON FOR EXECUTING ALL INSTRUCTIONS WITH THE TRACE BIT SET IS TO TAKE US INTO SERVICE AT THE END OF EACH INSTRUCTION.

THE CORE LAYOUT IS BROKEN INTO FIVE DISTINCT PARTS:

- (1) THE TRAP CATCHER,
- (2) THE SET UP AND I/O PRIMER AREA AND I/O TEST ROUTINES,
- (3) THE PROCESSOR TESTS AND
- (4) CONTROL AND UTILITY ROUTINES,
- (5) CORE DETECTOR AND EXPANSION ROUTINE.

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10. LISTING

11. FLOW CHART(S)

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561 .ENDR
562 .LIST SEQ,ME
563 .ABS
564 ;COPYRIGHT 1971, 1972, DIGITAL EQUIPMENT CORPORATION, MAYNARD MASS. 01754
565 ;PDP11 PRELIMINARY SYSTEM TEST --- TTY=PC11-LP11,RF11,TC11,KW11L,RK11,RC11,RP11 AND K-11
566 ;TEST SIMULTANEOUS RUNNING OF I/O, WITH PROCESSOR INSTRUCTION TEST AND WITH
567 ;WITH TRACE BIT ENABLED TO RE CONSIDER MAINLINE CODE
568 000240 NOP=240 ;SYSTEM NULL OPERATION
569 104000 HLT=EMT ;TRAP USED FOR ERROR PRINTOUT
570 104400 SCOPE=TRAP ;TRAP USED SCOPE LOOP AND ITERATION OF SUB PROBLEMS
571 177776 CC=177776
572 016022 TDSR=TCSR
573 016676 BUFF=FIN
574 177570 SR=177570
575 000000 R100=%0
576 000001 R101=%1
577 000002 RSR=%2
578 176000 RKWORDCT=-2000
579 176000 RPWORDCT=-2000
580 176040 RCWORDCT=-2000+40
581 176040 RFWORDCT=-2000+40
582 000000 XX=0
583 000000 .=0
584 .REPT 100 ;TRAP ENTRANCE
585 .+2 ;TRAPPED TO PREVIOUS LOCATION
586 HALT
587 .ENDR
588 000000 000002 .+2 ;TRAP ENTRANCE
589 000002 000000 HALT ;TRAPPED TO PREVIOUS LOCATION
590 000004 000006 .+2 ;TRAP ENTRANCE
591 000006 000000 HALT ;TRAPPED TO PREVIOUS LOCATION
592 000010 000012 .+2 ;TRAP ENTRANCE
593 000012 000000 HALT ;TRAPPED TO PREVIOUS LOCATION
594 000014 000016 .+2 ;TRAP ENTRANCE
595 000016 000000 HALT ;TRAPPED TO PREVIOUS LOCATION
596 000020 000022 .+2 ;TRAP ENTRANCE
597 000022 000000 HALT ;TRAPPED TO PREVIOUS LOCATION
598 000024 000026 .+2 ;TRAP ENTRANCE
599 000026 000000 HALT ;TRAPPED TO PREVIOUS LOCATION
600 000030 000032 .+2 ;TRAP ENTRANCE
601 000032 000000 HALT ;TRAPPED TO PREVIOUS LOCATION
602 000034 000036 .+2 ;TRAP ENTRANCE
603 000036 000000 HALT ;TRAPPED TO PREVIOUS LOCATION
604 000040 000042 .+2 ;TRAP ENTRANCE
605 000042 000000 HALT ;TRAPPED TO PREVIOUS LOCATION
606 000044 000046 .+2 ;TRAP ENTRANCE
607 000046 000000 HALT ;TRAPPED TO PREVIOUS LOCATION
608 000050 000052 .+2 ;TRAP ENTRANCE
609 000052 000000 HALT ;TRAPPED TO PREVIOUS LOCATION
610 000054 000056 .+2 ;TRAP ENTRANCE
611 000056 000000 HALT ;TRAPPED TO PREVIOUS LOCATION
612 000060 000062 .+2 ;TRAP ENTRANCE
613 000062 000000 HALT ;TRAPPED TO PREVIOUS LOCATION

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614	000064	000066	.+2	;TRAP ENTRANCE
615	000066	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
616	000070	000072	.+2	;TRAP ENTRANCE
617	000072	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
618	000074	000076	.+2	;TRAP ENTRANCE
619	000076	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
620	000100	000102	.+2	;TRAP ENTRANCE
621	000102	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
622	000104	000106	.+2	;TRAP ENTRANCE
623	000106	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
624	000110	000112	.+2	;TRAP ENTRANCE
625	000112	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
626	000114	000116	.+2	;TRAP ENTRANCE
627	000116	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
628	000120	000122	.+2	;TRAP ENTRANCE
629	000122	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
630	000124	000126	.+2	;TRAP ENTRANCE
631	000126	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
632	000130	000132	.+2	;TRAP ENTRANCE
633	000132	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
634	000134	000136	.+2	;TRAP ENTRANCE
635	000136	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
636	000140	000142	.+2	;TRAP ENTRANCE
637	000142	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
638	000144	000146	.+2	;TRAP ENTRANCE
639	000146	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
640	000150	000152	.+2	;TRAP ENTRANCE
641	000152	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
642	000154	000156	.+2	;TRAP ENTRANCE
643	000156	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
644	000160	000162	.+2	;TRAP ENTRANCE
645	000162	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
646	000164	000166	.+2	;TRAP ENTRANCE
647	000166	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
648	000170	000172	.+2	;TRAP ENTRANCE
649	000172	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
650	000174	000176	.+2	;TRAP ENTRANCE
651	000176	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
652	000200	000202	.+2	;TRAP ENTRANCE
653	000202	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
654	000204	000206	.+2	;TRAP ENTRANCE
655	000206	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
656	000210	000212	.+2	;TRAP ENTRANCE
657	000212	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
658	000214	000216	.+2	;TRAP ENTRANCE
659	000216	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
660	000220	000222	.+2	;TRAP ENTRANCE
661	000222	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
662	000224	000226	.+2	;TRAP ENTRANCE
663	000226	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
664	000230	000232	.+2	;TRAP ENTRANCE
665	000232	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
666	000234	000236	.+2	;TRAP ENTRANCE
667	000236	000000	HALT	;TRAPPED TO PREVIOUS LOCATION

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668	000240	000242	.+2	;TRAP ENTRANCE
669	000242	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
670	000244	000246	.+2	;TRAP ENTRANCE
671	000246	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
672	000250	000252	.+2	;TRAP ENTRANCE
673	000252	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
674	000254	000256	.+2	;TRAP ENTRANCE
675	000256	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
676	000260	000262	.+2	;TRAP ENTRANCE
677	000262	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
678	000264	000266	.+2	;TRAP ENTRANCE
679	000266	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
680	000270	000272	.+2	;TRAP ENTRANCE
681	000272	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
682	000274	000276	.+2	;TRAP ENTRANCE
683	000276	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
684	000300	000302	.+2	;TRAP ENTRANCE
685	000302	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
686	000304	000306	.+2	;TRAP ENTRANCE
687	000306	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
688	000310	000312	.+2	;TRAP ENTRANCE
689	000312	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
690	000314	000316	.+2	;TRAP ENTRANCE
691	000316	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
692	000320	000322	.+2	;TRAP ENTRANCE
693	000322	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
694	000324	000326	.+2	;TRAP ENTRANCE
695	000326	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
696	000330	000332	.+2	;TRAP ENTRANCE
697	000332	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
698	000334	000336	.+2	;TRAP ENTRANCE
699	000336	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
700	000340	000342	.+2	;TRAP ENTRANCE
701	000342	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
702	000344	000346	.+2	;TRAP ENTRANCE
703	000346	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
704	000350	000352	.+2	;TRAP ENTRANCE
705	000352	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
706	000354	000356	.+2	;TRAP ENTRANCE
707	000356	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
708	000360	000362	.+2	;TRAP ENTRANCE
709	000362	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
710	000364	000366	.+2	;TRAP ENTRANCE
711	000366	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
712	000370	000372	.+2	;TRAP ENTRANCE
713	000372	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
714	000374	000376	.+2	;TRAP ENTRANCE
715	000376	000000	HALT	;TRAPPED TO PREVIOUS LOCATION
716	000014		.=14	
717	000014	000016	.+2	
718	000016	000000	HALT	
719	000030		.=30	
720	000030	015540	PRINT	
721	000032	000340	340	

;FALSE TRACE TRAP
;FOR HALT TRAPS
;HIGHEST PRIORITY

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722 000034 .=34
723 000034 016324 SCOPEC ;USER TRAP
724 000036 000000 2
725
726 100200 .=200
727 ;(R6) IS THE STACK POINTER
728 ;((R6)) IS THE PC+2 OF LOCATION WHERE THE TRAP ORIGINATED
729 ;FOR NORMAL OPERATION RUN WITH ALL SWITCHES DOWN
730 ;SR 15=1 OR UP---HALT ON ERROR
731 ;SR 14=1 OR UP---SCOPE LOOP
732 ;SR 13=1 OR UP---INHIBIT PRINT OUT
733 ;SR 12=1 OR UP---INHIBIT TRACE TRAPPING
734 ;SR 11=1 OR UP---INHIBIT SUB-PROBLEM ITERATION
735 ;SR 10=1 OR UP---INHIBIT PROCESSOR TEST
736 ;SR 09=1 OR UP INHIBIT VARIABLE CORE EXPANSION
737 ;SR 08=1 OR UP RESTART ON ERROR
738 ;SPECIAL DELETE SWITCHES-SET RESPECTIVE SWITCH TO A 1 TO INHIBIT INITIATION OF DEVICE
739
740 ;SW 0=1 INHIBIT TTY OUTPUT
741 ;SW 1=1 INHIBIT TTY INPUT
742 ;SW 2=1 INHIBIT HSP
743 ;SW 3=1 INHIBIT HSR
744 ;SW 4=1 INHIBIT LINE CLOCK
745 ;SW 5=1 INHIBIT RC, FF, RK, RP DISKS
746 ;SW 6=1 INHIBIT TC11 DECTAPE
747 ;SW 7=1 INHIBIT LINE PRINTER --- IF LINE PRINTER IS USED, MUST RESTART AT 500
748 ;IF EAE EXIST IT WILL BE AUTOMATICALLY SELECTED,
749 ;POP11 SIMULTANEOUS I/O
750 000060 .=60
751 000060 001364 TTYINR ;TTY IN INTERRUPT VECTOR
752 000062 000200 200
753 000064 001440 TTYOUTR ;TTY OUT INTERRUPT VECTOR
754 000066 000200 200
755 000070 001466 HSRINR ;HSR INTERRUPT VECTOR
756 000072 000200 200
757 000074 001560 HPOUTR ;HSP INTERRUPT VECTOR
758 000076 000200 200
759 000100 .=100
760 000100 001664 LK3 ;INTERRUPT VECTOR LINE CLOCK
761 000102 000300 300 ;LEVEL SIX PRIORITY
762
763 000200 .=200
764 000200 000137 000502 JMP @#START
765 000204 .=204
766 000204 002450 IRF ;RF11 DISK
767 000206 000240 240 ;LEVEL 5
768 000210 002352 IRC ;RC DISK
769 000212 000240 240
770
771 000214 .=214
772 000214 002534 FENDZ ;DEC TAPE
773 000216 000300 300 ;LEVEL 5
774 000220 .=220
775 000220 002164 IRK ;RK DISK

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776	000222	000240	240	
777				
778		000254	*254	
779	000254	000266	IRP	
780	000256	000240	240	;RP DISK
781				
782		177776	STATUS=177776	
783	000260	177560	TRCSR: 177560	
784	000262	177562	TRDRI: 177562	
785	000264	177564	TTCSR: 177564	
786	000266	177566	TTDBR: 177566	
787	000270	177550	HRCSR: 177550	
788	000272	177552	HRDBR: 177552	
789	000274	177554	HPCSR: 177554	
790	000276	177556	HPDBR: 177556	
791	000300	177546	LKCSR: 177546	
792	000302	177514	LPCSR: 177514	
793	000304	177516	LPDBR: 177516	
794	000306	177470	RFDAE: 177470	IDISK ADDRESS AND ERROR
795	000310	177466	RFDAR: 177466	IDISK ADDRESS REGISTER
796	000312	177462	RFWCI: 177462	IWORD COUNT REGISTER
797	000314	177464	RFCAR: 177464	ICURRENT ADDRESS REGISTER
798	000316	177460	RFCSR: 177460	ISTATUS REGISTER
799	000320	177461	RFCSRH: 177461	IHIGH BYTE ADDRESS OR CSR
800	000322	177442	RCDAR: 177442	IDISK ADDRESS REGISTER
801	000324	177450	RCWCI: 177450	IWORD COUNT REGISTER
802	000326	177452	RCBAR: 177452	ICURRENT ADDRESS REGISTER
803	000330	177446	RCCSR: 177446	ISTATUS REGISTER
804	000332	177447	RCCSRH: 177447	IHIGH BYTE ADDRESS OR CSR
805	000334	177413	RKDAH: 177413	IHIGH BYTE OF DISK ADDRESS
806	000336	177412	RKDAE: 177412	IDISK ADDRESS REGISTER
807	000340	177406	RKWCI: 177406	IWORD COUNT REGISTER
808	000342	177410	RKBAR: 177410	ICURRENT ADDRESS REGISTER
809	000344	177404	RKCSR: 177404	ISTATUS REGISTER
810	000346	177405	RKCSRH: 177405	IHIGH BYTE ADDRESS OR CSR
811	000350	177304	MQ: 177304	IEAE LOCATIONS
812	000352	177302	AC: 177302	
813	000354	177310	SC: 177310	
814	000356	177311	SRE: 177311	
815	000360	177306	MUL: 177306	
816	000362	177300	DIV: 177300	
817	000364	177312	NOR: 177312	
818	000366	177314	LSH: 177314	
819	000370	177316	ASH: 177316	
820				
821			DECTAPE ADDRESSES	
822		177340	TC=177340	
823	000372	177342	TCCM: TC+2	ICONTROL AND FUNCTION
824	000374	177340	TCSTI: TC	IGENERAL STATUS
825	000376	177350	TCDTI: TC+10	
826	000400	000440	BR START	IDATA
827	000402	177344	TCWCI: TC+4	IWORD COUNT
828	000404	177346	TCBAI: TC+6	IBUS ADDRESS
829	000406	000214	TCIVI: 214	IDECTAPE INTERRUPT VECTOR

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830 000410 176722 RPCAI 176722 ;CYLINDER ADDRESS RP11 DISK
831 000412 176725 RPDAH: 176725 ;HIGH BYTE OF DISK ADDRESS
832 000414 176724 RPDAE: 176724 ;DISK ADDRESS
833 000416 176710 RPDAR: 176724 ;DRIVE STATUS REGISTER
834 000420 176724 RPDAR: 176724 ;DISK ADDRESS REGISTER
835 000422 176716 RPWC1 176716 ;WORD COUNT REGISTER
836 000424 176720 RPBAR: 176720 ;CURRENT ADDRESS REGISTER
837 000426 176714 RPCSR: 176714 ;STATUS REGISTER
838 000430 176715 RPCSRH: 176715 ;HIGH BYTE ADDRESS OR CSR
839 000432 000000 RPFUNCTION: 0 ;DISK COMMAND
840 ;THIS ROUTINE CHECKS THE READ DATA BUFFER TC11
841 ;BY DOING A CHECK SUM ON THE DATA
842 000434 010146 TC1: MOV %1,-(6) ;SAVE THESE ON THE STACK
843 000436 010346 MOV %3,-(6)
844 000440 005003 CLR %3 ;SUM OF DATA
845 000442 012701 003256 MOV #TCRBUF,%1 ;ADDRESS OF READ BUFFER
846 000446 062103 TC2: ADD (1)+,%3 ;EVEN ADD
847 000450 062103 ADD (1)+,%3 ;ODD ADD -2'S COMPLIMENT
848 000452 001775 REQ TC2
849 000454 020127 004256 CMP %1,#TCRBUF+1000 ;AT END OF BUFFER?
850 000460 101001 RHI .+4 ;YES BRANCH
851 000462 104000 HLT ;DATA ERROR
852 000464 012603 MOV (6)+,%3 ;RESTORE THE REGISTERS
853 000466 012601 MOV (6)+,%1
854 000470 000207 RTS %7 ;EXIT
855 000472 012767 000240 014206 NOEAE: MOV #240.EAESRT ;BRANCH AROUND EAE ROUTINE
856 000500 000002 RTI ;JUMP OVER EAE SECTION
857
858 ;START UP FOR MINI MONITOR
859
860 000502 016767 177052 000652 START: MOV SR,REG1 ;MOV SR TO REGISTER
861 000510 005067 015654 ESTART: CLR ICOUNT
862 000514 012706 016676 MOV #BUFF,%6 ;SET UP STACK
863 000520 012767 000556 015656 MOV #START2,RETURN
864 000526 005067 015650 CLR SCOPEF
865 000532 012767 000340 177236 MOV #340.STATUS ;LOCK OUT INTERRUPTS
866 000540 005067 014772 CLR PRFLAG ;PRINT ROUTINE BUSY
867 000544 016702 000612 MOV REG1.RSR ;SAVE SWITCHES
868 000550 005067 177014 CLR SR ;FOR 11/45 DISPLAY
869 000554 012700 000100 MOV #100,R100 ;INTERRUPT ENABLE
870 000560 012701 000101 MOV #101,R101 ;INTERRUPT ENABLE AND GO
871 000564 104400 SCOPE
872 000566 050077 177456 START2: BIS R100,@TRCSR
873 000572 000005 RESET
874 000574 030077 177450 BIT R100,@TRCSR ;INTERRUPT ENABLE
875 000600 001401 REQ .+4
876 000602 104000 HLT ;RESET DID NOT CLEAR INTERRUPT ENABLE
877 000604 104400 SCOPE
878 ;DOES "RESET" ON THE BUS LAST TOO LONG
879 000606 012706 016676 MOV #BUFF,%6 ;SET UP STACK
880 000612 000005 RESET
881 000614 050077 177444 BIS R100,@TTCSR ;SET A BIT
882 000620 030077 177440 RIT R100,@TTCSR ;IS IT SET
883 000624 001001 BNE .+4

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884 000626 104000 HLT ;RESET IS ON BUS TOO LONG
885 000630 104400 SCOPE
886 000632 050077 177426 BIS R100, @TTCSR
887 000636 005077 177422 CLR @TTCSR
888 000642 104400 SCOPE
889 000644 000005 RESET
890 000646 012767 004272 015530 MOV #BEGIN, RETURN
891 000654 012737 000472 000004 MOV #NOEAE, @#4
892 000662 005777 177452 TST @MO
893 000666 012767 000006 177110 MOV #6, 4
894 000674 012767 000002 177104 MOV #2, 6
895 000702 012767 000001 000526 MOV #1, DATA1
896 000710 005067 000530 CLR DATA2
897 000714 012767 000001 000616 MOV #1, DATA3
898 000722 005067 000706 CLR DATA4
899 000726 012706 016676 MOV #BUFF, X6
900 000732 005067 000702 CLR DELAY
901 000736 012767 000340 177032 MOV #340, STATUS
902 000744 030227 000001 BIT RSR, #1
903 000750 001002 BNE ST1
904 000752 050077 177306 BIS R100, @TTCSR ;TTY OUT
905 000756 030227 000002 ST1: BIT RSR, #2
906 000762 001002 BNE ST2
907 000764 050177 177270 BIS R101, @TRCSR ;TTY IN
908 000770 005777 177300 ST2: TST @HPCSR ;TEST FOR OUT OF TAPE
909 000774 100405 BMI ST3
910 000776 030227 000004 BIT RSR, #4
911 001002 001002 BNE ST3
912 001004 050077 177254 BIS R100, @HPCSR ;HSP
913 001010 005777 177254 ST3: TST @HRCSR ;TEST FOR OUT OF TAPE
914 001014 100407 BMI ST4
915 001016 030227 000010 BIT RSR, #10
916 001022 001004 BNE ST4
917 001024 010067 000610 MOV R100, DELAY ;FOR STALL HSR
918 001030 050177 177234 BIS R101, @HRCSR ;HSR
919 001034 030227 000020 ST4: BIT RSR, #20
920 001040 001004 BNE ST5
921 001042 005067 000712 CLR TIME
922 001046 050077 177226 BIS R100, @LKCSR ;LINE CLOCK 50 OR 60 CYCLES
923 001052 030227 000040 ST5: BIT RSR, #40
924 001056 001050 BNE ST6
925 001060 012767 001122 176716 MOV #ST5A, 4
926 001066 105777 177334 TSTB @RPCSR ;WAIT FOR CONTROLLER READY
927 001072 100375 BPL .-4
928 001074 012777 000015 177324 MOV #15, @RPCSR ;RESET DRIVE
929 001102 105777 177320 TSTB @RPCSR ;WAIT FOR CONTROLLER READY
930 001106 100375 BPL .-4
931 001110 005777 177302 TST @RPDSR ;WAIT FOR ACCESS READY
932 001114 100375 BPL .-4
933 001116 005077 177274 CLR @RPDSR ;CLR ATTENTION
934 001122 012767 000006 176654 ST5AB MOV #6, 4
935 001130 012767 043503 001362 MOV #43503, RFFUNCTION ;WRITE CHECK/ WRITE RF
936 001136 012767 043503 001244 MOV #43503, RCFUNCTION
937 001144 012767 043503 001054 MOV #43503, RKFUNCTION

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938	001152	012767	043583	177252	MOV	#43583,RPFUNCTION	
939	001160	110077	177132		MOVB	R100,@RFCSR	;TELL DISK TO READ OR WRITE
940	001164	110077	177154		MOVB	R100,@RKCSR	
941	001170	110077	177134		MOVB	R100,@RCCSR	
942	001174	110077	177226		MOVB	R100,@RPCSR	
943	001200	030200		ST6:	BIT	RSR,R100	
944	001202	001011			RNE	ST7	;TEST FOR DECTAPE
945	001204	012767	002524	001320	MOV	#TCFIRST,TGEXPE	
946	001212	012777	002534	177166	MOV	#FENDZ,@TCIV	
947	001220	012777	004183	177144	MOV	#R+IE+RB+DD,@TCCM	
948	001226	105722		ST7:	TSTB	RSR	
949	001230	130427			BMI	ST8	
950	001232	012767	001310	176544	MOV	#ST8,4	
951	001240	012767	000137	000662	MOV	#137,SOLPAT	
952	001246	012767	000117	000656	MOV	#79,,CLINCT	
953	001254	012767	000137	000644	MOV	#137,CURPAT	
954	001262	012777	000014	177014	MOV	#14,@LPDRR	
955	001270	012737	002026	000200	MOV	#LPIINTR,@#200	
956	001276	012737	000200	000202	MOV	#200,@#202	
957	001304	010077	176772		MOV	R100,@LPCSR	
958	001310	005037	015524	ST8:	CLR	@#TRPB	
959	001314	004737	016780		JSR	%7,%#USER	
960	001320	004767	015356		JSR	%7,DFT1	
961	001324	005067	176456		CLR	6	
962	001330	012767	000006	176446	MOV	#6,4	
963	001336	005067	176434		CLR	STATUS	
964	001342	000401			RR	.+4	
965	001344	000001		MAINLINE:	WAIT		;WAIT HERE FOR INTERRUPT
966	001346	036727	176216	002000	BIT	SR,#2000	;INHIBIT PROCESSOR TEST
967	001354	001373			RNE	MAINLINE	
968	001356	000167	002710		JMP	REGIN	
969	001362	000000		REG11:	0		:STATUS OF SELECTED DEVICES
970							
971							
972	001364	105777	176670		TTYINR:	TSTB @TRCSH	
973	001370	100401				RMI .+4	
974	001372	104000				HLT	
975	001374	105777	176652			TSTB @TRDR	
976	001400	001413				REQ TTYIN2	
977	001402	127767	176654	000026		CMPB @TRDR,DATA1	
978	001410	001401				REQ TTYIN3	
979	001412	104000				HLT	
980	001414	105267	000016		TTYIN3:	INC B DATA1	
981	001420	001003				TTYIN4: BNE TTYIN2	
982	001422	012767	000001	000006	TTYIN1:	MOV #1,DATA1	
983	001430	005277	176624		TTYIN2:	INC @TRCSR	
984	001434	000002				RTI	
985							
986	001436	000000			DATA1:	XX	
987							
988							
989							
990	001440	105777	176620		TYOUTR:	TSTB @TCSR	
991	001444	100401				BMI .+4	

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992 001446 104000 HLT ;FALSE INTERRUPT RETURN
993 001450 105267 000010 INCB ;INCREMENT DATA
994 001454 016777 000004 176604 TYOUT1: MOV ;OUTPUT TO DEVICE
995 001462 000002 RTI ;RETURN TO MAINLINE
996
997 001464 000000 DATA2: XX ;TRANSMITTED DATA
998 ;HSR SECTION VALUES 0 TO 377
999
1000 001466 105777 176576 HSRINR: TSTB @HRCsr ;IS DONE SET
1001 001472 100401 BMI .+4
1002 001474 104000 HLT ;FALSE RETURN FROM MAINLINE
1003 001476 105777 176570 TSTB @HRDBR ;TEST DATA FOR LEADER
1004 001502 001413 BEQ HSRIN2 ;IF LEADER GO BACK
1005 001504 127767 176562 000026 CMPB @HRDBR,DATA3 ;NOT LEADER TEST FOR DATA
1006 001512 001401 REQ .+4
1007 001514 104000 HLT ;DATA COMPARISON ERROR
1008 001516 105267 000016 INCB DATA3 ;INCREMENT DATA
1009 001522 001003 BNE HSRIN2
1010 001524 012767 000001 000006 HSRIN1: MOV #1,DATA3 ;BASE DATA
1011 001532 005277 176532 HSRIN2: INC @HRCsr ;START READER
1012 001536 000002 RTI ;RETURN TO MAINLINE
1013
1014 001540 000000 DATA3: XX ;EXPECTED DATA
1015
1016 ;HS PUNCH SECTION, VALUES 0 TO 377
1017 ;ENABLE READER ON FIX COUNT OF PUNCH ONLY (14 TIMES)
1018 001542 012767 000000 000064 HPOUT: MOV #0,DATA4 ;INITIAL DATA
1019 001550 016777 000000 176520 HPOUT1: MOV DATA4,@HPDPR ;OUTPUT TO DEVICE
1020 001556 000002 RTI ;RETURN TO MAINLINE
1021 001560 105777 176510 HPOUTR: TSTB @HPCsr ;TEST FOR DONE
1022 001564 100401 BMI .+4
1023 001566 104000 HLT ;FALSE INTERRUPT RETURN
1024 001570 046777 000044 176472 BIC DELAY,@HRCsr ;CLEAR HSR INTERRUPT ENABLE
1025 001576 005267 000034 INC INTCNT ;COUNT INTERRUPTS
1026 001602 026727 000030 000014 CMP INTCNT,#14 ;SAVE TO TURN READER ON?
1027 001610 001005 BNE HPOUT2 ;NO-NEED MORE TIME
1028 001612 005067 000020 CLR INTCNT ;YES RESET COUNTER
1029 001616 056777 000016 176444 BIS DELAY,@HRCsr ;SET READER INT ENABLE
1030 001624 105267 000004 HPOUT2: INCB DATA4 ;INCREMENT DATA
1031 001630 001744 REQ HPOUT ;AT UPPER LIMIT START OVER
1032 001632 000746 BR HPOUT1 ;FINISH REST OF DATA
1033
1034 001634 000000 DATA4: XX
1035 001636 000000 INTCNT: 0
1036 001640 000000 DELAY: 0 ;EQUAL 100 IF HSR RUNNING
1037
1038 ;TEST OF LINE CLOCK, INTERRUPT FOR 55 SECONDS THEN STALL FOR 5 SECONDS.
1039 001642 005037 001760 LK1: CLR #TIME ;CLEAR LINE CLOCK TIMER
1040 001646 052777 000100 176424 BIS #100,@LKCSR
1041 001654 052767 000100 176114 BIS #100,STATUS
1042 001662 000002 LK2: RTI ;RETURN TO MAINLINE
1043 001664 105777 176410 LK3: TSTB @LKCSR ;TEST FOR DONE
1044 001670 100401 BMI .+4
1045 001672 104000 HLT ;FALSE INTERRUPT

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1046 001674 042777 000200 176376 BIC #200,@LKCSR
1047 001702 005237 001750 LK4: INC @#TIME
1048 001706 022737 006344 001760 CMP #3320.,@#TIME
1049 001714 103362 RHIS LK2 :BRANCH IF TIME LESS THAN 35 SECONDS
1050 001716 042777 000100 176354 BIC #102,@LKCSR
1051 001724 042767 000100 176044 RIC #102,STATUS
1052 001732 022737 007020 001760 CMP #3620.,@#TIME
1053 001740 001740 BEQ LK1 :YES-RESET TIMER
1054 001742 105777 176332 TSTB @LKCSR :NO-SKIP ON FLAG TILL IT IS.
1055 001746 100375 BPL .-4
1056 001750 042777 000200 176322 RIC #200,@LKCSR ;CLEAR THE FLAG
1057 001756 000751 BR LK4 ;FOUND FLAG GO INCREMENT COUNTER
1058 001760 000000 TIME: @
1059
1060 . ;LINE PRINTER SHOULD RAISE PROCESSOR PRIORITY TO LEVEL OF LINE PRINTER
1061 ;INTERRUPT VECTOR IS 200
1062
1063 001762 016767 000142 000136 LP1: MOV SOLPAT,CURPAT ;START OF LINE TO CURRENT
1064 001770 016777 000132 176306 LP2: MOV CURPAT,@LPDDR ;CURRENT PATTERN TO LINE PRINTER
1065 001776 105777 176300 TSTB @LPCSR
1066 002002 100405 BMI LP6
1067 002004 000002 RTI ;RETURN TO MAIN LINE
1068 002006 105777 176270 LPINTR: TSTB @LPCSR ;TEST FOR FLAG
1069 002012 100401 PMI .+4
1070 002014 104000 HLT
1071 002016 026727 000110 000117 LP6: CMP CLINCT,#79, ;FALSE RETURN FROM MAIN LINE
1072 ;TEST FOR END OF LINE,
;CHANGE THIS VALUE FOR 132 COLUMN PRINTERS
;GO GENERATE CR/LF
1073 002024 001415 REQ LP4
1074 002026 005267 000100 INC CLINCT ;INCREMENT LINE POSITION COUNT
1075 002032 026727 000070 000137 CMP CURPAT,#137 ;TEST FOR MAXIMUM PATTERN
1076 002040 001403 REQ LP3 ;YES = GO TO LP3 AND RESET
1077 002042 005267 000050 INC CURPAT ;NO - INCREMENT TO NEXT PATTERN
1078 002046 000750 BR LP2 ;GO SEND IT TO LINE PRINTER
1079 002050 012767 000040 000050 LP3: MOV #40,CURPAT ;RESET PATTERN AND SEND TO PRINTER
1080 002056 000744 PR LP2 ;SENT TO LINE PRINTER
1081 002060 005067 000046 LP4: CLR CLINCT ;RESET LINE COUNT
1082 002064 012777 000012 176212 MOV #12,@LPDDR ;LINE FEED
1083 002072 105777 176274 TSTB @LPCSR
1084 002076 100375 BPL .-4
1085 002100 026727 000024 000137 CMP SOLPAT,#137 ;START OF LINE PATTERN
1086 002106 001403 BEQ LP5
1087 002110 005267 000014 INC SOLPAT ;INCREMENT START OF LINE
1088 002114 000722 BR LP1
1089 002116 012767 000040 000004 LP5: MOV #40,SOLPAT ;RESET START OF LINE
1090 002124 000716 BR LP1 ;PRINT
1091 002126 000000 CURPAT: @ ;CURRENT CHARACTER BEING PRINTED
1092 002130 000000 SOLPAT: @ ;START OF LINE CHARACTER
1093 002132 000000 CLINCT: @ ;POSITION OF LINE
1094
1095 ;RK11 DISK TEST INTERRUPT LEVEL 5, 2000 WORD TRANSFERS
1096 002134 005077 176176 RKSTART: CLR @RKDAE ;INITIALIZE DISK = DAR-DAE
1097 002140 016777 000356 176174 RK1: MOV LLIMIT,@RKBAR ;CORE BASE
1098 002146 012777 176000 176164 MOV #RKWORDCT,@RKWC ;LENGTH OF TRANSFER
1099 002154 113777 002226 176162 MOVB @#RKFUNCTION,@RKCSR ;WRITE OR WRITE CHECK TO DISK

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1100 002162 000002 RTI ;RETURN TO MAINLINE CODE
1101 002164 032777 100200 176152 IRK: BIT #100200, @RKCSR ;INTERRUPT VECTOR POINTS HERE
1102 002172 003002 BGT .+6
1103 002174 104000 HLT
1104 002176 000756 BR RKSTART
1105 002200 032777 000037 176130 BIT #37, @RKDAE ;RK-11 ERROR FLAG UP OR READY NOT UP
1106 002206 001354 BNE RK1 ;NO
1107 002210 122777 000031 176116 CMPB #31, @RKDAH
1108 002216 001350 BNE RK1 ;NO
1109 002220 000337 002226 SWAB @#RKFUNCTION ;CHANGE COMMAND
1110 002224 000743 BR RKSTART ;RESTART NEW TRANSFER OF DISK
1111
1112 002226 000000 RKFUNCTION: 0 ;DISK COMMAND
1113 002230 105277 176172 ;RP11 DISK SERVICE ROUTINE
1114 002234 105777 176166 RPSTART: INCB @RPCSR ;INITIALIZE DISK - DAR=DAE
1115 002240 100375 TSTB @RPCSR
1116 002242 016777 000254 176154 RP1: BPL .-4
1117 002250 012777 176000 176144 MOV LLIMIT, @RPBAR ;INITIAL CORE ADDRESS
1118 002256 113777 000432 176142 MOV #RPWORDCT, @RPWC ;LENGTH OF TRANSFER
1119 002264 000002 MOVB @#RPFUNCTION, @RPCSR ;WRITE OR WRITE CHECK TO DISK
1120 002266 032777 100200 176132 IRP: RTI ;RETURN TO MAINLINE CODE
1121 002274 003002 BIT #100200, @RPCSR ;INTERRUPT VECTOR POINTS HERE
1122 002276 104000 BGT .+6
1123 002300 000753 HLT
1124 002302 122777 000312 176100 BR RPSTART ;RP11 READY NOT UP OR ERROR
1125 002310 001354 CMPB #312, @RPCA ;CYLINDER NO. 312
1126 002312 000367 176114 BNE RP1 ;NO
1127 002316 000744 SWAB RPFUNCTION ;CHANGE COMMAND
1128 002320 012777 000040 175774 ;RC11 DISK SERVICE ROUTINE
1129 002326 016777 000170 175772 RCSTART: MOV #40, @RCDDR ;INITIALIZE DISK - DAR=DAE
1130 002334 012777 176040 175762 RC2: MOV LLIMIT, @RCBAR ;CORE BASE
1131 002342 113777 002410 175760 MOV #RCWORDCT, @RCWC ;LENGTH OF TRANSFER
1132 002350 000002 MOVB @#RCFUNCTION, @RCCSR ;WRITE OR WRITE CHECK TO DISK
1133 002352 037727 175752 100200 IRC: RTI ;RETURN TO MAINLINE CODE
1134 002360 003002 BIT @RCCSR, #100200 ;INTERRUPT VECTOR POINTS HERE
1135 002362 104000 BGT .+6
1136 002364 000755 HLT
1137 002366 005277 175730 BR RCSTART ;RC11 READY NOT UP OR ERROR IS UP
1138 002372 022777 002000 175722 INC @RCDDR ;TO INCREASE XFER RATE
1139 002400 001352 CMP #2000, @RCDDR ;DISK AT UPPER LIMIT, 4000=2, 6000=3, 12000=4
1140 002402 000337 002410 BNE RC2 ;NO
1141 002406 000744 SWAB @#RCFUNCTION ;CHANGE COMMAND
1142 002410 000000 BR RCSTART ;RESTART NEW TRANSFER OF DISK
1143 002412 105277 175702 RCFUNCTION: 0 ;DISK COMMAND
1144 002416 062777 000040 175664 ;IRF11 DISK
1145 002424 016777 000072 175662 RFSTART: INCB @RFCCSRH ;INITIALIZE DISK - DAR=DAE
1146 002432 012777 176040 175652 ADD #40, @RFDDR ;INCREASE DUTY CYCLE
1147 002440 113777 002520 175650 RF1: MOV LLIMIT, @RFCAR ;CORE BASE
1148 002446 000002 BNE RF2: MOV #RFWORDCT, @RFWC ;LENGTH OF TRANSFER
1149 002450 037727 175642 100200 IRF: MOVB @#RFFUNCTION, @RFCCSR ;WRITE OR WRITE CHECK TO DISK
1150 002456 003002 RTI ;RETURN TO MAINLINE CODE
1151 002466 000000 BIT @RFCCSR, #100200 ;INTERRUPT VECTOR POINTS HERE
1152 002472 000000 BGT .+6

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1154 002460 104000 HLT ;RF11 READY NOT UP OR ERROR UP
1155 002462 000753 RR RESTART
1156 002464 062777 000040 175616 ADD #40, @RFDAR ;INCREASE DUTY CYCLE
1157 002472 122777 000003 175606 CMPB #3, @RFDAE ;DISK AT UPPER LIMIT? 7=2, 17=4, 37=8
1158 002500 001351 BNE RF1 ;NO
1159 002502 027727 175622 174000 CMP @RFDAR, #174000 ;AS FAR ON DISK AS WE CAN GO
1160 002510 101745 BLDS RF1 ;NO
1161 002512 000337 002520 SWAB @#RFFUNCTION ;CHANGE COMMAND
1162 002516 000735 RR RESTART ;RESTART NEW TRANSFER OF DISK
1163 002520 000000 RFFUNCTION: @ ;DISK COMMAND
1164 002522 004272 LLIMIT: BEGIN ;FIRST CORE ADDRESS OF TRANSFER
1165 :DT11 DEC TAPE
1166 000004 RD=4 ;READ DATA
1167 000014 WD=14 ;WRITE DATA
1168 000002 RB=2
1169 000002 BR=2 ;READ BLOCK
1170 000000 F=0 ;FORWARD
1171 000100 IE=100 ;INTERRUPT ENABLE
1172 000001 DO=1 ;DO - THE FUNCTION
1173 004000 R=4000 ;REVERSE
1174
1175 002524 000000 TCFIRST: 0 ;FIRST BLOCK TO BE SEARCHED FOR
1176 002526 001101 TCLAST: 577. ;LAST BLOCK TO BE SEARCHED FOR
1177 002530 000000 TCBLK: @ ;CURRENT BLOCK FOUND
1178 002532 000000 TCEXPE: @ ;THE BLOCK THAT IS EXPECTED
1179
1180 :GO TO FORWARD END ZONE
1181 002534 012777 002534 175644 FENDZ: MOV #FENDZ, @TCIV ;END ZONE VECTOR SETUP
1182 002542 005777 175626 TST @TCST ;TEST FOR END ZONE
1183 002546 100403 BMI FEND1 ;AT END ZONE?
1184 002550 105277 175616 INCB @TCM ;SET DO - NO DELAY
1185 002554 000002 RTI ;NO - WAIT SOME MORE
1186 002556 012777 002606 175622 FEND1: MOV #TCF1, @TCIV ;YES - NEW VECTOR
1187 002564 042777 104000 175600 BIC #104000, @TCM ;SEARCH BLOCK FORWARD
1188 002572 016767 177726 177732 MOV TCFIRST, TCEXPE ;COUNT WHEN THIS BLOCK IS FOUND
1189 002600 105277 175566 TCF1A: INCB @TCM ;SET DO
1190 002604 000002 RTI ;RETURN ON NEXT BLOCK
1191 002606 032777 100200 175556 TCF1I: BIT #100200, @TCM ;ANY ERROR ON READ?
1192 002614 003001 BGT .+4
1193 002616 104000 HLT ;TC ERROR SET - FORWARD READ BLOCK
1194 002620 027767 175552 177704 CMP @TCDT, TCEXPE ;IS THIS OUR BLOCK FOR SYNC
1195 002626 002764 BLT TCF1A ;NO-READ SOME MORE BLOCKS
1196 002630 001401 BEQ TCF2 ;YES
1197 002632 104000 HLT ;WE PASSED THE BLOCK
1198
1199 002634 012777 002650 175544 TCF2I: MOV #TCF3, @TCIV ;VECTOR FOR SEQUENTIAL READS
1200 002642 105277 175524 INCB @TCM ;SET DO
1201 002646 000002 RTI ;RETURN AND TEST SEQUENTIAL BLOCKS
1202
1203 :FIND SEQUENTIAL BLOCK AT FORWARD DIRECTION
1204 002650 032777 100200 175514 TCF3I: BIT #100200, @TCM ;TEST ERROR AND READY
1205 002656 003001 BGT .+4
1206 002660 104000 HLT ;FALSE INTERRUPT ON TC-11
1207 002662 027767 175510 177636 CMP @TCDT, TCLAST ;HAVE WE TESTED ALL BLOCKS

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1208 002670 001414 BEQ RENDZ ;YES DRIVE UNIT IN END ZONE TO START OVER
1209 002672 005267 177634 INC TCEXPE ;NO-INCREMENT EXPECTED COUNT
1210 002676 027767 175474 177626 CMP @TCDT,TCEXPE ;IS CURRENT BLOCK CORRECT
1211 002704 001401 BEQ .+4
1212 002706 104000 HLT ;FAILED IN FOWARD READ TO FIND NEXT BLOCK
1213 002710 000427 BR TCWBK ;THIS ROUTINE WRITES A BLOCK
1214 002712 105277 175454 TCF4I INCB @TCCM ;SET DO
1215 002716 000002 RTI
1216 002720 000705 XFENDZ: BR FENDZ ;INDIRECT LINK
1217
1218 ;MOVE TAPE TO REVERSE END ZONE
1219 002722 012777 002722 175456 RENDZ: MOV #RENDZ,@TCIV ;END ZONE VECTOR SETUP
1220 002730 016767 177572 177574 MOV TCLAST,TCEXPE ;SET UP FOR REVERSE SEARCH
1221 002736 005777 175432 TST @TCST ;IN END ZONE
1222 002742 100403 BMI REND1 ;YES - START TO TURN UNIT AROUND
1223 002744 105277 175422 INCB @TCCM ;SET DO
1224 002750 000002 RTI ;NO - WAIT TILL WE ARE
1225 002752 012777 004103 175412 REND1: MOV #R+IE+RB+DO,@TCCM ;FUNCTION = READ BLOCK, REVERSE AND GO
1226 002760 012777 003050 175420 MOV #TCR1,@TCIV ;SET UP NEW INTERRUPT VECTOR
1227 002766 000002 RTI
1228 ;WRITE FORWARD ALL BLOCKS EXCEPT 0
1229
1230 002770 012777 003022 175410 TCWBK: MOV #TCWB1,@TCIV ;INTERRUPT VECTOR FOR WRITE
1231 002776 012777 177400 175376 MOV #-402,@TCWC ;ONE BLOCK
1232 003004 012777 003256 175372 MOV #TCWRUF,@TCBA ;THE WRITE BUFFER ADDRESS
1233 003012 112777 000115 175352 MOVB #IE+WD+DO,@TCCM ;WRITE THE BLOCK
1234 003020 000002 RTI ;RETURN WHEN BLOCK IS WRITTEN
1235 003022 005777 175344 TCWB1: TST @TCCM ;ANY ERRORS
1236 003026 100001 BPL .+4
1237 003030 104000 HLT
1238 003032 012777 002650 175346 MOV #TCF3,@TCIV ;SEARCH BLOCK VECTOR
1239 003040 112777 000102 175324 MOVB #IE+RB,@TCCM ;READ BLOCK
1240 003046 000721 BR TCF4 ;FIND THE NEXT BLOCK
1241
1242 003050 032777 100200 175314 TCR1I: BIT #100200,@TCCM ;TEST FOR ERROR AND READY
1243 003056 003001 BGT .+4
1244 003060 104000 HLT
1245 003062 027767 175310 177442 CMP @TCDT,TCEXPE ;DECTAPE ERROR ON READ BLOCK REVERSE
1246 003070 001406 BEQ TCR2 ;IS IT OUR FIRST BLOCK
1247 003072 002002 BGE TCR1A ;YES - GO TEST THE REST
1248 003074 104000 HLT ;NO - HAVE WE PASSED THE BLOCK
1249 003076 000711 BR RENDZ ;WE PASS OUR BLOCK
1250 003100 105277 175266 TCR1A: INCB @TCCM ;GO TO END ZONE AND TRY AGAIN
1251 003104 000002 RTI ;SET DO
1252 003106 012777 003122 175272 TCR2I: MOV #TCR3,@TCIV ;WE FOUND OUR FIRST BLOCK
1253 003114 105277 175252 INCB @TCCM ;SET UP INTERRUPT TO TEST ALL BLOCKS
1254 003120 000002 RTI ;SET DO
1255 ;WAIT FOR NEXT BLOCK TO INTERRUPT
1256 ;FIND SEQUENTIAL BLOCK IN REVERSE DIRECTION
1257 003122 032777 100200 175242 TCR3I: BIT #100200,@TCCM ;TEST FOR READ AND ERROR
1258 003130 003001 BGT .+4
1259 003132 104000 HLT ;ERROR READING SEQUENTIAL BLOCK IN REVERSE
1260 003134 026777 177354 175234 CMP TCFIRST,@TCDT ;DID WE DO ALL THE BLOCKS
1261 003142 001666 BEQ XFENDZ ;YES - GO TO END ZONE TO RESTART

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1262 003144 005367 177362 DEC TCEXPE INO = DECREMENT BLOCK NUMBER
1263 003150 027767 175222 177354 CMP @TCCT, TCEXPE ;TEST SEQUENTAIL BLOCK IN REVERSE
1264 003156 001401 REQ .+4
1265 003160 104000 HLT
1266 003162 000403 RR TCRBK ;TEST SECENTIAL READ BLOCK IN REVERSE FAILED
1267 003164 105277 175202 TCR41 INCB @TCCM ;THIS ROUTINE READ A BLOCK
1268 003170 000002 RTI ;SET DO
1269
1270 ;READ REVERSE ALL BLOCK EXCEPT BLOCK 1121
1271 003172 012777 003230 175206 TCRBK: MOV #TCR#1, @TCIV ;SET UP INTERRUPT VECTOR
1272 003200 012777 177400 175174 MOV #-400, @TCWC ;READ ONE BLOCK
1273 003206 012777 003256 175170 MOV #TCRFUF, @TCBA ;WHERE BUFFER IS
1274 003214 112777 000105 175150 MOVB #IE+RD+00, @TCCM ;READ THE BLOCK
1275 003222 004767 175226 JSR %7,T@1 ;CHECK DATA BUFFER
1276 003226 000002 RTI ;EXIT = RETURN WHEN BLOCK IS READ
1277 003230 005777 175136 TCRB1: TST @TCCM ;HAND ERRORS
1278 003234 100001 BPL .+4
1279 003236 104000 HLT
1280 003240 012777 003122 175140 MOV #TCR3, @TCIV ;NEW VECTOR FOR BLOCK SEARCH
1281 003246 112777 000102 175116 MOVB #IE+RB, @TCCM ;READ BLOCK FUNCTION
1282 003254 000743 BR TCR4 ;RETURN TO BLOCK SEARCH
1283
1284 ;THIS WRITE BUFFER LOOK THE SAME FORWARD OR REVERSE
1285 003256 TCWRBUF:
1286 003256 TCRBUF:
1287 000001 N=1
1288 .REPT 100
1289 N ;DECTAPE READ/WRITE BUFFER
1290 -N
1291 N=N+1
1292 .ENDR
1293 003256 000001 N ;DECTAPE READ/WRITE BUFFER
1294 003260 177777 -N
1295 000002 N=N+1
1296 003262 000002 N ;DECTAPE READ/WRITE BUFFER
1297 003264 177776 -N
1298 000003 N=N+1
1299 003266 000003 N ;DECTAPE READ/WRITE BUFFER
1300 003270 177775 -N
1301 000004 N=N+1
1302 003272 000004 N ;DECTAPE READ/WRITE BUFFER
1303 003274 177774 -N
1304 000005 N=N+1
1305 003276 000005 N ;DECTAPE READ/WRITE BUFFER
1306 003300 177773 -N
1307 000006 N=N+1
1308 003302 000006 N ;DECTAPE READ/WRITE BUFFER
1309 003304 177772 -N
1310 000007 N=N+1
1311 003306 000007 N ;DECTAPE READ/WRITE BUFFER
1312 003310 177771 -N
1313 000010 N=N+1
1314 003312 000010 N ;DECTAPE READ/WRITE BUFFER
1315 003314 177770 -N

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1316	000011		
1317	003316	000011	N=N+1
1318	003320	177767	N
1319		000012	-N
1320	003322	000012	N=N+1
1321	003324	177766	N
1322		000013	-N
1323	003326	000013	N=N+1
1324	003330	177765	N
1325		000014	-N
1326	003332	000014	N=N+1
1327	003334	177764	N
1328		000015	-N
1329	003336	000015	N=N+1
1330	003340	177763	N
1331		000016	-N
1332	003342	000016	N=N+1
1333	003344	177762	N
1334		000017	-N
1335	003346	000017	N=N+1
1336	003350	177761	N
1337		000018	-N
1338	003352	000018	N=N+1
1339	003354	177760	N
1340		000019	-N
1341	003356	000019	N=N+1
1342	003360	177757	N
1343		000020	-N
1344	003362	000020	N=N+1
1345	003364	177756	N
1346		000021	-N
1347	003366	000021	N=N+1
1348	003370	177755	N
1349		000022	-N
1350	003372	000022	N=N+1
1351	003374	177754	N
1352		000023	-N
1353	003376	000023	N=N+1
1354	003400	177753	N
1355		000024	-N
1356	003402	000024	N=N+1
1357	003404	177752	N
1358		000025	-N
1359	003406	000025	N=N+1
1360	003410	177751	N
1361		000026	-N
1362	003412	000026	N=N+1
1363	003414	177750	N
1364		000027	-N
1365	003416	000027	N=N+1
1366	003420	177747	N
1367		000028	-N
1368	003422	000028	N=N+1
1369	003424	177746	N
			-N

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1370	003426	000033	N=N+1	;DECTAPE READ/WRITE BUFFER
1371	003426	000033	N	
1372	003430	177745	-N	
1373		000034	N=N+1	
1374	003432	000034	N	;DECTAPE READ/WRITE BUFFER
1375	003434	177744	-N	
1376		000035	N=N+1	
1377	003436	000035	N	;DECTAPE READ/WRITE BUFFER
1378	003440	177743	-N	
1379		000036	N=N+1	
1380	003442	000036	N	;DECTAPE READ/WRITE BUFFER
1381	003444	177742	-N	
1382		000037	N=N+1	
1383	003446	000037	N	;DECTAPE READ/WRITE BUFFER
1384	003450	177741	-N	
1385		000040	N=N+1	
1386	003452	000040	N	;DECTAPE READ/WRITE BUFFER
1387	003454	177740	-N	
1388		000041	N=N+1	
1389	003456	000041	N	;DECTAPE READ/WRITE BUFFER
1390	003460	177737	-N	
1391		000042	N=N+1	
1392	003462	000042	N	;DECTAPE READ/WRITE BUFFER
1393	003464	177736	-N	
1394		000043	N=N+1	
1395	003466	000043	N	;DECTAPE READ/WRITE BUFFER
1396	003470	177735	-N	
1397		000044	N=N+1	
1398	003472	000044	N	;DECTAPE READ/WRITE BUFFER
1399	003474	177734	-N	
1400		000045	N=N+1	
1401	003476	000045	N	;DECTAPE READ/WRITE BUFFER
1402	003500	177733	-N	
1403		000046	N=N+1	
1404	003502	000046	N	;DECTAPE READ/WRITE BUFFER
1405	003504	177732	-N	
1406		000047	N=N+1	
1407	003506	000047	N	;DECTAPE READ/WRITE BUFFER
1408	003510	177731	-N	
1409		000050	N=N+1	
1410	003512	000050	N	;DECTAPE READ/WRITE BUFFER
1411	003514	177730	-N	
1412		000051	N=N+1	
1413	003516	000051	N	;DECTAPE READ/WRITE BUFFER
1414	003520	177727	-N	
1415		000052	N=N+1	
1416	003522	000052	N	;DECTAPE READ/WRITE BUFFER
1417	003524	177726	-N	
1418		000053	N=N+1	
1419	003526	000053	N	;DECTAPE READ/WRITE BUFFER
1420	003530	177725	-N	
1421		000054	N=N+1	
1422	003532	000054	N	;DECTAPE READ/WRITE BUFFER
1423	003534	177724	-N	

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1424		000055	N=N+1	
1425	003536	000055	N	;DECTAPE READ/ WRITE BUFFER
1426	003540	177723	-N	
1427		000056	N=N+1	
1428	003542	000056	N	;DECTAPE READ/ WRITE BUFFER
1429	003544	177722	-N	
1430		000057	N=N+1	
1431	003546	000057	N	;DECTAPE READ/ WRITE BUFFER
1432	003550	177721	-N	
1433		000060	N=N+1	
1434	003552	000060	N	;DECTAPE READ/ WRITE BUFFER
1435	003554	177720	-N	
1436		000061	N=N+1	
1437	003556	000061	N	;DECTAPE READ/ WRITE BUFFER
1438	003560	177717	-N	
1439		000062	N=N+1	
1440	003562	000062	N	;DECTAPE READ/ WRITE BUFFER
1441	003564	177716	-N	
1442		000063	N=N+1	
1443	003566	000063	N	;DECTAPE READ/ WRITE BUFFER
1444	003570	177715	-N	
1445		000064	N=N+1	
1446	003572	000064	N	;DECTAPE READ/ WRITE BUFFER
1447	003574	177714	-N	
1448		000065	N=N+1	
1449	003576	000065	N	;DECTAPE READ/ WRITE BUFFER
1450	003600	177713	-N	
1451		000066	N=N+1	
1452	003602	000066	N	;DECTAPE READ/ WRITE BUFFER
1453	003604	177712	-N	
1454		000067	N=N+1	
1455	003606	000067	N	;DECTAPE READ/ WRITE BUFFER
1456	003610	177711	-N	
1457		000070	N=N+1	
1458	003612	000070	N	;DECTAPE READ/ WRITE BUFFER
1459	003614	177710	-N	
1460		000071	N=N+1	
1461	003616	000071	N	;DECTAPE READ/ WRITE BUFFER
1462	003620	177707	-N	
1463		000072	N=N+1	
1464	003622	000072	N	;DECTAPE READ/ WRITE BUFFER
1465	003624	177706	-N	
1466		000073	N=N+1	
1467	003626	000073	N	;DECTAPE READ/ WRITE BUFFER
1468	003630	177705	-N	
1469		000074	N=N+1	
1470	003632	000074	N	;DECTAPE READ/ WRITE BUFFER
1471	003634	177704	-N	
1472		000075	N=N+1	
1473	003636	000075	N	;DECTAPE READ/ WRITE BUFFER
1474	003640	177703	-N	
1475		000076	N=N+1	
1476	003642	000076	N	;DECTAPE READ/ WRITE BUFFER
1477	003644	177702	-N	

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1478	000077	N=N+1		
1479	003646	000077	N	;DECTAPE READ/WRITE BUFFER
1480	003650	177701	-N	
1481		000100	N=N+1	
1482	003652	000100	N	;DECTAPE READ/WRITE BUFFER
1483	003654	177700	-N	
1484		000101	N=N+1	
1485			,REPT 100	
1486			N=N-1	
1487			-N	
1488			N	;DEC TAPE READ/WRITE BUFFER
1489			.ENDR	
1490		000100	N=N-1	
1491	003656	177700	-N	
1492	003660	000100	N	;DEC TAPE READ/WRITE BUFFER
1493		000077	N=N-1	
1494	003662	177701	-N	
1495	003664	000077	N	;DEC TAPE READ/WRITE BUFFER
1496		000076	N=N-1	
1497	003666	177702	-N	
1498	003670	000076	N	;DEC TAPE READ/WRITE BUFFER
1499		000075	N=N-1	
1500	003672	177703	-N	
1501	003674	000075	N	;DEC TAPE READ/WRITE BUFFER
1502		000074	N=N-1	
1503	003676	177704	-N	
1504	003700	000074	N	;DEC TAPE READ/WRITE BUFFER
1505		000073	N=N-1	
1506	003702	177705	-N	
1507	003704	000073	N	;DEC TAPE READ/WRITE BUFFER
1508		000072	N=N-1	
1509	003706	177706	-N	
1510	003710	000072	N	;DEC TAPE READ/WRITE BUFFER
1511		000071	N=N-1	
1512	003712	177707	-N	
1513	003714	000071	N	;DEC TAPE READ/WRITE BUFFER
1514		000070	N=N-1	
1515	003716	177710	-N	
1516	003720	000070	N	;DEC TAPE READ/WRITE BUFFER
1517		000067	N=N-1	
1518	003722	177711	-N	
1519	003724	000067	N	;DEC TAPE READ/WRITE BUFFER
1520		000066	N=N-1	
1521	003726	177712	-N	
1522	003730	000066	N	;DEC TAPE READ/WRITE BUFFER
1523		000065	N=N-1	
1524	003732	177713	-N	
1525	003734	000065	N	;DEC TAPE READ/WRITE BUFFER
1526		000064	N=N-1	
1527	003736	177714	-N	
1528	003740	000064	N	;DEC TAPE READ/WRITE BUFFER
1529		000063	N=N-1	
1530	003742	177715	-N	
1531	003744	000063	N	;DEC TAPE READ/WRITE BUFFER

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1532	000062	N=N-1	
1533	003746	-N	
1534	003750	N	;DEC TAPE READ/WRITE BUFFER
1535	000062	N=N-1	
1536	003752	-N	
1537	003754	N	;DEC TAPE READ/WRITE BUFFER
1538	000061	N=N-1	
1539	003756	-N	
1540	003760	N	;DEC TAPE READ/WRITE BUFFER
1541	000060	N=N-1	
1542	003762	-N	
1543	003764	N	;DEC TAPE READ/WRITE BUFFER
1544	000057	N=N-1	
1545	003766	-N	
1546	003770	N	;DEC TAPE READ/WRITE BUFFER
1547	000056	N=N-1	
1548	003772	-N	
1549	003774	N	;DEC TAPE READ/WRITE BUFFER
1550	000055	N=N-1	
1551	003776	-N	
1552	004000	N	;DEC TAPE READ/WRITE BUFFER
1553	000054	N=N-1	
1554	004002	-N	
1555	004004	N	;DEC TAPE READ/WRITE BUFFER
1556	000053	N=N-1	
1557	004006	-N	
1558	004010	N	;DEC TAPE READ/WRITE BUFFER
1559	000052	N=N-1	
1560	004012	-N	
1561	004014	N	;DEC TAPE READ/WRITE BUFFER
1562	000051	N=N-1	
1563	004016	-N	
1564	004020	N	;DEC TAPE READ/WRITE BUFFER
1565	000050	N=N-1	
1566	004022	-N	
1567	004024	N	;DEC TAPE READ/WRITE BUFFER
1568	000049	N=N-1	
1569	004026	-N	
1570	004030	N	;DEC TAPE READ/WRITE BUFFER
1571	000048	N=N-1	
1572	004032	-N	
1573	004034	N	;DEC TAPE READ/WRITE BUFFER
1574	000047	N=N-1	
1575	004036	-N	
1576	004040	N	;DEC TAPE READ/WRITE BUFFER
1577	000046	N=N-1	
1578	004042	-N	
1579	004044	N	;DEC TAPE READ/WRITE BUFFER
1580	000045	N=N-1	
1581	004046	-N	
1582	004050	N	;DEC TAPE READ/WRITE BUFFER
1583	000044	N=N-1	
1584	004052	-N	
1585	004054	N	;DEC TAPE READ/WRITE BUFFER

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1586	000040	N=N-1	
1587	004056	177740	-N
1588	004060	000040	N
1589		000037	N=N-1 ;DEC TAPE READ/WRITE BUFFER
1590	004062	177741	-N
1591	004064	000037	N
1592		000036	N=N-1 ;DEC TAPE READ/WRITE BUFFER
1593	004066	177742	-N
1594	004070	000036	N
1595		000035	N=N-1 ;DEC TAPE READ/WRITE BUFFER
1596	004072	177743	-N
1597	004074	000035	N
1598		000034	N=N-1 ;DEC TAPE READ/WRITE BUFFER
1599	004076	177744	-N
1600	004100	000034	N
1601		000033	N=N-1 ;DEC TAPE READ/WRITE BUFFER
1602	004102	177745	-N
1603	004104	000033	N
1604		000032	N=N-1 ;DEC TAPE READ/WRITE BUFFER
1605	004106	177746	-N
1606	004110	000032	N
1607		000031	N=N-1 ;DEC TAPE READ/WRITE BUFFER
1608	004112	177747	-N
1609	004114	000031	N
1610		000030	N=N-1 ;DEC TAPE READ/WRITE BUFFER
1611	004116	177750	-N
1612	004120	000030	N
1613		000027	N=N-1 ;DEC TAPE READ/WRITE BUFFER
1614	004122	177751	-N
1615	004124	000027	N
1616		000026	N=N-1 ;DEC TAPE READ/WRITE BUFFER
1617	004126	177752	-N
1618	004130	000026	N
1619		000025	N=N-1 ;DEC TAPE READ/WRITE BUFFER
1620	004132	177753	-N
1621	004134	000025	N
1622		000024	N=N-1 ;DEC TAPE READ/WRITE BUFFER
1623	004136	177754	-N
1624	004140	000024	N
1625		000023	N=N-1 ;DEC TAPE READ/WRITE BUFFER
1626	004142	177755	-N
1627	004144	000023	N
1628		000022	N=N-1 ;DEC TAPE READ/WRITE BUFFER
1629	004146	177756	-N
1630	004150	000022	N
1631		000021	N=N-1 ;DEC TAPE READ/WRITE BUFFER
1632	004152	177757	-N
1633	004154	000021	N
1634		000020	N=N-1 ;DEC TAPE READ/WRITE BUFFER
1635	004156	177760	-N
1636	004160	000020	N
1637		000017	N=N-1 ;DEC TAPE READ/WRITE BUFFER
1638	004162	177761	-N
1639	004164	000017	;DEC TAPE READ/WRITE BUFFER

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1640	000016	N=N-1			
1641	004166	177762	-N		
1642	004170	000016	N		
1643		000015	N=N-1		
1644	004172	177763	-N		
1645	004174	000015	N		
1646		000014	N=N-1		
1647	004176	177764	-N		
1648	004200	000014	N		
1649		000013	N=N-1		
1650	004202	177765	-N		
1651	004204	000013	N		
1652		000012	N=N-1		
1653	004206	177766	-N		
1654	004210	000012	N		
1655		000011	N=N-1		
1656	004212	177767	-N		
1657	004214	000011	N		
1658		000010	N=N-1		
1659	004216	177770	-N		
1660	004220	000010	N		
1661		000007	N=N-1		
1662	004222	177771	-N		
1663	004224	000007	N		
1664		000006	N=N-1		
1665	004226	177772	-N		
1666	004230	000006	N		
1667		000005	N=N-1		
1668	004232	177773	-N		
1669	004234	000005	N		
1670		000004	N=N-1		
1671	004236	177774	-N		
1672	004240	000004	N		
1673		000003	N=N-1		
1674	004242	177775	-N		
1675	004244	000003	N		
1676		000002	N=N-1		
1677	004246	177776	-N		
1678	004250	000002	N		
1679		000001	N=N-1		
1680	004252	177777	-N		
1681	004254	000001	N		
1682			;DEC TAPE READ/WRITE BUFFER		
1683	004256	122727	000000 000001	CMPB #0,#1	;T7 FIX
1684	004264	002401		BLT .+4	;CMPB FAILED
1685	004266	104000		HLT	
1686	004270	104400		SCOPE	
1687	004272	012767	004272 012104	BEGIN: MOV #BEGIN,RETURN	;FOR SCOPING
1688	004300	104400		SCOPE	
1689	004302	012737	004000 016400	MOV #4000,@#ICOUNT	;ITERATION COUNT
1690				;TEST COMPARE INSTRUCTION INDEXED	
1691	004310	012700	177770	MOV #-10,%0	;MINUS 10 TO REG 0
1692	004314	026027	016602 125252	CMP A(0),#125252	;A INDEX BY MINUS 10) TO #125252
1693	004322	001401		BEQ .+4	

1694 004324 104000 HLT ;COMPARE WITH INDEX FAILED
1695 004326 104400 SCOPE
1696
1697 004330 012700 177770 MOV #-10,%0 ;FOR INDEX
1698 004334 022760 125252 016602 CMP #125252,A(0) ;A INDEXED
1699 004342 001401 BEQ .+4
1700 004344 104000 HLT ;COMPARE FAILED DESTINATION INDEX
1701 004346 104400 SCOPE
1702 ;SET "ISR" FOR DISKS AND KW11L TO CURRENT BANK
1703 004350 010700 MOV %7,%0 ;CURRENT BANK
1704 004352 042700 007777 RIC #007777,%0 ;LEAVE ONLY BANK BITS
1705 004356 062700 001654 ADD #LK3,%0 ;ADD IN CLOCK ENTRANCE
1706 004362 010037 000100 MOV %0,%#100 ;LINE CLOCK, KW11L
1707 004366 042700 007777 RIC #007777,%0
1708 004372 062700 002450 ADD #IRF,%0
1709 004376 010037 000204 MOV %0,%#204 ;RF11 ISR
1710 004402 042700 007777 RIC #007777,%0
1711 004406 062700 002352 ADD #IRC,%0
1712 004412 010037 000210 MOV %0,%#210 ;RC11, ISR
1713 004416 042700 007777 RIC #007777,%0
1714 004422 062700 002154 ADD #IRK,%0
1715 004426 010037 000220 MOV %0,%#220 ;RK11 ISR
1716 004432 042700 007777 BIC #7777,%0
1717 004436 062700 002256 ADD #IRP,%0
1718 004442 010037 000254 MOV %0,%#254 ;RP11 ISR
1719 004446 042700 007777 RIC #007777,%0
1720 004452 063700 002522 ADD @#LLIMIT,%0
1721 004456 010067 176040 MOV %0,LLIMIT ;CHANGE DISK NPR BUFFER
1722 004462 042700 007777 RIC #007777,%0
1723 004466 062700 016676 ADD #BUFF,%0
1724 004472 010006 MOV %0,%6 ;CHANGE STACK TO EXISTING BANK
1725
1726 004474 012700 000010 MOV #10,%0 ;INDEX
1727 004500 026027 016602 052525 CMP A(0),#052525
1728 004506 001401 BEQ .+4
1729 004510 104000 HLT ;COMPARE FAILED
1730 004512 104400 SCOPE
1731
1732 004514 012700 000010 MOV #10,%0
1733 004520 022760 052525 016602 CMP #052525,A(0)
1734 004526 001401 BEQ .+4
1735 004530 104000 HLT ;COMPARE FAILED
1736 004532 104400 SCOPE
1737
1738 004534 012700 177770 MOV #-10,%0
1739 004540 026060 016602 016602 CMP A(0),A(0)
1740 004546 001401 BEQ .+4
1741 004550 104000 HLT ;COMPARE FAILED
1742 004552 104400 SCOPE
1743
1744 004554 012700 000010 MOV #+10,%0
1745 004560 026060 016602 016602 CMP A(0),A(0)
1746 004566 001401 BEQ .+4
1747 004570 104000 HLT ;COMPARE FAILED

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1748 004572 104400 SCOPE
1749
1750 004574 012700 177770 MOV #-10,%0
1751 004600 012701 000004 MOV #+4,%1
1752 004604 026061 016602 016602 CMP A(0),A(1)
1753 004612 001401 BEQ .+4
1754 004614 104000 HLT ;COMPARE FAILED
1755 004616 104400 SCOPE
1756
1757 004620 026160 016602 016602 CMP A(1),A(0)
1758 004626 001401 BEQ .+4
1759 004630 104000 HLT ;COMPARE FAILED
1760 004632 104400 SCOPE
1761
1762 004634 012700 177774 MOV #-4,%0
1763 004640 012701 000010 MOV #+10,%1
1764 004644 026061 016602 016602 CMP A(0),A(1)
1765 004652 001401 BEQ .+4
1766 004654 104000 HLT ;CMP FAILED
1767 004656 104400 SCOPE
1768 004660 012700 177774 MOV #-4,%0
1769 004664 012701 000010 MOV #10,%1
1770 004670 026160 016602 016602 CMP A(1),A(0)
1771 004676 001401 BEQ .+4
1772 004700 104000 HLT ;COMPARE FAILED
1773 004702 104400 SCOPE
1774 :TEST MOVE INSTRUCTION FOR INDEX
1775
1776 004704 012700 177770 MOV #-10,%0
1777 004710 016067 016602 011706 MOV A(0),TEMP
1778 004716 026727 011702 125252 CMP TEMP,#125252
1779 004724 001401 BEQ .+4
1780 004726 104000 HLT ;COMPARE FAILED
1781 004730 104400 SCOPE
1782
1783 004732 012700 000010 MOV #+10,%0
1784 004736 016067 016602 011660 MOV A(0),TEMP
1785 004744 026727 011654 052525 CMP TEMP,#052525
1786 004752 001401 BEQ .+4
1787 004754 104000 HLT ;MOV FAILED
1788 004756 104400 SCOPE
1789
1790 004760 012700 177770 MOV #-10,%0
1791 004764 012760 125252 016624 MOV #125252,TEMP(0)
1792 004772 023727 016614 125252 CMP @#C,#125252

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1793 005000 001401 REQ .+4
1794 005002 104000 HLT ;MOV FAILED
1795 005004 104400 SCOPE
1796
1797 005006 012700 000010 MOV #+10,%0
1798 005012 012700 052525 016624 MOV #052525,TEMP(0)
1799 005020 023727 016634 052525 CMP @#TEMP+10,#052525
1800 005026 001401 REQ .+4
1801 005030 104000 HLT ;MOV FAILED
1802 005032 104400 SCOPE
1803
1804 :TEST BIC INSTRUCTION FOR INDEXING
1805 005034 012767 177777 011562 MOV #-1,TEMP
1806 005042 012700 177770 MOV #-10,%0
1807 005046 046067 016622 011550 RIC A(0),TEMP
1808 005054 026727 011544 052525 CMP TEMP,#052525
1809 005062 001401 REQ .+4
1810 005064 104000 HLT ;BIC FAILED
1811 005066 104400 SCOPE
1812
1813 005070 012767 177777 011526 MOV #-1,TEMP
1814 005076 012700 000010 MOV #10,%0
1815 005102 046067 016632 011514 RIC A(0),TEMP
1816 005110 026727 011510 125252 CMP TEMP,#125252
1817 005116 001401 REQ .+4
1818 005120 104000 HLT ;BIC FAILED
1819 005122 104400 SCOPE
1820
1821 005124 012737 177777 016634 MOV #-1,@#TEMP+10
1822 005132 012700 000010 MOV #10,%0
1823 005136 042760 125252 016624 RIC #125252,TEMP(0)
1824 005144 023727 016634 052525 CMP @#TEMP+10,#52525
1825 005152 001401 REQ .+4
1826 005154 104000 HLT ;BIC FAILED
1827 005156 104400 SCOPE
1828
1829 005160 012700 177770 MOV #-10,%0
1830 005164 012767 177777 011422 MOV #-1,TEMP-10
1831 005172 042767 052525 011414 RIC #052525,TEMP-10
1832 005200 026727 011410 125252 CMP TEMP-10,#125252
1833 005206 001401 REQ .+4
1834 005210 104000 HLT ;BIC FAILED
1835 005212 104400 SCOPE
1836 :TEST SUBTRACT INSTRUCTION FOR INDEXING
1837 005214 012767 125252 011402 MOV #125252,TEMP
1838 005222 012700 177770 MOV #-10,%0
1839 005226 005226 016602 011370 SUB A(0),TEMP
1840 005234 001401 REQ .+4
1841 005236 104000 HLT ;SUB FAILED
1842 005240 104400 SCOPE
1843
1844 005242 012737 125252 016624 MOV #125252,@#TEMP
1845 005250 012700 177770 MOV #-10,%0
1846 005254 166760 011312 016634 SUB B,TEMP+10(0)

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1847 005262 001401 BEQ .+4
1848 005264 104000 HLT
1849 005266 104400 SCOPE ;SUB FAILED
1850
1851 005270 012767 052525 011326 MOV #052525,TEMP
1852 005276 012700 000010 MOV #10,%0
1853 005302 166067 016602 011314 SUB A(0),TEMP
1854 005310 001421 BEQ .+4
1855 005312 104000 HLT
1856 005314 104400 SCOPE ;SUB FAILED
1857
1858 005316 012737 052525 016624 MOV #052525,@#TEMP
1859 005324 012700 000010 MOV #10,%0
1860 005330 166760 011256 016614 SUB A+10.C(0)
1861 005336 001401 REQ .+4
1862 005340 104000 HLT
1863 005342 104400 SCOPE ;SUB FAILED
1864
1865 ;TEST UNARYS INDEXED
1866 005344 012737 177777 016624 MOV #-1,@#TEMP
1867 005352 012700 177770 MOV #-10,%0
1868 005356 005060 016634 CLR D(0)
1869 005362 005737 016624 TST @#TEMP
1870 005366 001401 BEQ .+4
1871 005370 104000 HLT
1872 005372 104400 SCOPE ;CLR FAILED
1873
1874 005374 012737 177777 016624 MOV #-1,@#TEMP
1875 005402 012700 000010 MOV #+10.%0
1876 005406 005060 016614 CLR C(0)
1877 005412 005737 016624 TST @#TEMP
1878 005416 001401 BEQ .+4
1879 005420 104000 HLT
1880 005422 104400 SCOPE ;CLR FAILED
1881
1882 005424 012737 177777 016624 MOV #-1,@#TEMP
1883 005432 012700 177770 MOV #-10,%0
1884 005436 005160 016634 COM D(0)
1885 005442 005737 016624 TST @#TEMP
1886 005446 001401 REQ .+4
1887 005450 104000 HLT
1888 005452 104400 SCOPE ;COM FAILED
1889
1890 005454 012737 177777 016624 MOV #-1,@#TEMP
1891 005462 012700 000010 MOV #10,%0
1892 005466 005160 016614 COM C(0)
1893 005472 005737 016624 TST @#TEMP
1894 005476 001401 BEQ .+4
1895 005500 104000 HLT
1896 005502 104400 SCOPE ;COM FAILED
1897 005504 012737 177777 016624 MOV #-1,@#TEMP
1898 005512 012700 177770 MOV #-10.%0
1899 005516 005260 016634 INC D(0)
1900 005522 005737 016624 TST @#TEMP

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1901	005526	001401		BEQ	.+4	
1902	005530	104000		HLT		;INC FAILED
1903	005532	104400		SCOPE		
1904						
1905	005534	012737	177777	016624	MOV	#-1,@#TEMP
1906	005542	012700	000010		MOV	#+10,%0
1907	005546	005260	016614		INC	C(0)
1908	005552	005737	016624		TST	@#TEMP
1909	005556	001401			REQ	.+4
1910	005560	104000			HLT	
1911	005562	104400			SCOPE	
1912						
1913	005564	012737	000021	016624	MOV	#1,@#TEMP
1914	005572	012700	177770		MOV	#-10,%0
1915	005576	005360	016634		DEC	D(0)
1916	005602	005737	016624		TST	@#TEMP
1917	005606	001401			REQ	.+4
1918	005610	104000			HLT	
1919	005612	104400			SCOPE	
1920						
1921	005614	012737	000021	016624	MOV	#1,@#TEMP
1922	005622	012700	000010		MOV	#10,%0
1923	005626	005360	016614		DEC	C(0)
1924	005632	005737	016624		TST	@#TEMP
1925	005636	001401			REQ	.+4
1926	005640	104000			HLT	
1927	005642	104400			SCOPE	
1928						
1929	005644	012737	000021	016624	MOV	#1,@#TEMP
1930	005652	012700	177770		MOV	#-10,%0
1931	005656	005460	016634		NEG	D(0)
1932	005662	022737	177777	016624	CMP	#-1,@#TEMP
1933	005670	001401			REQ	.+4
1934	005672	104000			HLT	
1935	005674	104400			SCOPE	
1936						
1937	005676	012737	000021	016624	MOV	#1,@#TEMP
1938	005704	012700	000010		MOV	#+10,%0
1939	005710	005460	016614		NEG	C(0)
1940	005714	022737	177777	016624	CMP	#-1,@#TEMP
1941	005722	001401			REQ	.+4
1942	005724	104000			HLT	
1943	005726	104400			SCOPE	
1944						
1945	005730	012737	177777	016624	MOV	#-1,@#TEMP
1946	005736	012700	177770		MOV	#-10,%0
1947	005742	000261			SEC	
1948	005744	005560	016634		ADC	D(0)
1949	005750	005737	016624		TST	@#TEMP
1950	005754	001401			REQ	.+4
1951	005756	104000			HLT	
1952	005760	104400			SCOPE	
1953						
1954	005762	012737	177777	016624	MOV	#-1,@#TEMP

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1955 005770 012700 000010 MOV #+10,%0
1956 005774 000261 SEC
1957 005776 005560 016614 ADC C(0)
1958 006002 005737 016624 TST @#TEMP
1959 006006 001401 BEQ .+4
1960 006010 104000 HLT ;ADC FAILED
1961 006012 104400 SCOPE
1962
1963 006014 012737 000031 016624 MOV #1,@#TEMP
1964 006022 012700 177770 MOV #-12,%0
1965 006026 000261 SEC
1966 006030 005560 016634 SBC D(0)
1967 006034 005737 016624 TST @#TEMP
1968 006040 001401 BEQ .+4
1969 006042 104000 HLT ;SBC FAILED
1970 006044 104400 SCOPE
1971
1972 006046 012737 000031 016624 MOV #1,@#TEMP
1973 006054 012700 000010 MOV #+10,%0
1974 006060 000261 SEC
1975 006062 005560 016614 SBC C(0)
1976 006066 005737 016624 TST @#TEMP
1977 006072 001401 BEQ .+4
1978 006074 104000 HLT ;SBC FAILED
1979 006076 104400 SCOPE
1980
1981 ;TEST JMP INDIRECT
1982 006100 010700 MOV %7,%0
1983 006102 002700 000010 ADD #10,%0
1984 006106 000110 JMP @%0
1985 006110 104000 HLT ;JMP FAILED
1986 006112 000240 NOP
1987 006114 104400 SCOPE
1988
1989 006116 010600 MOV %6,%0
1990 006120 010001 MOV %0,%1
1991 006122 010102 MOV %1,%2
1992 006124 010203 MOV %2,%3
1993 006126 010304 MOV %3,%4
1994 006130 010405 MOV %4,%5
1995 006132 020605 CMP %6,%5
1996 006134 001401 BEQ .+4
1997 006136 104000 HLT ;MOV REGISTER FAILED
1998 006140 104400 SCOPE
1999 ;TEST INDIRECT ADDRESSING
2000 ;TEST COMPARE INSTRUCTION
2001 006142 023727 016572 125252 CMP @#B,#125252
2002 006150 001401 BEQ .+4
2003 006152 104000 HLT ;CMP FAILED
2004 006154 104400 SCOPE
2005
2006 006156 022737 125252 016572 CMP #125252,@#B
2007 006164 001401 BEQ .+4
2008 006166 104000 HLT ;CMP FAILED

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2029 006170 104400 SCOPE
2010
2011 006172 023737 016572 016572 CMP @#B,@#B
2012 006200 001401 BEQ .+4 ;CMP FAILED
2013 006202 104000 HLT
2014 006204 104400 SCOPE
2015
2016 ;TEST MOVE INSTRUCTIONS
2017 006206 013700 016572 MOV @#B,%0
2018 006212 022700 125252 CMP #125252,%0
2019 006216 001401 BEQ .+4 ;MOV FAILED
2020 006220 104000 HLT
2021 006222 104400 SCOPE
2022
2023 006224 012737 125252 016624 MOV #125252,@#TEMP
2024 006232 023737 016572 016624 CMP @#B,@#TEMP
2025 006240 001401 BEQ .+4 ;MOV FAILED
2026 006242 104000 HLT
2027 006244 104400 SCOPE
2028
2029 006246 013737 016572 016614 MOV @#B,@#C
2030 006254 023737 016572 016614 CMP @#B,@#C
2031 006262 001401 BEQ .+4 ;MOV FAILED
2032 006264 104000 HLT
2033 006266 104400 SCOPE
2034 ;TEST BIC INSTRUCTION INDIRECT
2035 006270 012700 177777 MOV #-1,%0
2036 006274 043700 016572 BIC @#B,%0
2037 006300 020027 052525 CMP %0,#052525
2038 006304 001401 BEQ .+4 ;BIC FAILED
2039 006306 104000 HLT
2040 006310 104400 SCOPE
2041
2042 006312 012737 177777 016624 MOV #-1,@#TEMP
2043 006320 042737 125252 016624 BIC #125252,@#TEMP
2044 006326 022737 052525 016624 CMP #052525,@#TEMP
2045 006334 001401 BEQ .+4 ;BIC FAILED
2046 006336 104000 HLT
2047 006340 104400 SCOPE
2048
2049 006342 012737 177777 016614 MOV #-1,@#C
2050 006350 043737 016572 016614 BIC @#B,@#C
2051 006356 023727 016614 052525 CMP @#C,#52525
2052 006364 001401 BEQ .+4 ;BIC FAILED
2053 006366 104000 HLT
2054 006372 104400 SCOPE
2055
2056 ;TEST SUBTRACT INSTRUCTION
2057 006372 012700 125252 MOV #125252,%0
2058 006376 163700 016572 SUB @#B,%0
2059 006402 020027 000000 CMP %0,%0
2060 006406 001401 BEQ .+4 ;SUB FAILED
2061 006410 104000 HLT
2062 006412 104400 SCOPE

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2063
2064 006414 012737 125252 016624 MOV #125252,@#TEMP
2065 006422 166737 010144 016624 SUB B,@#TEMP
2066 006430 001401 REQ ,+4
2067 006432 104000 HLT
2068 006434 104400 SCOPE ;SUB FAILED
2069
2070 006436 012767 125252 010160 MOV #125252,TEMP
2071 006444 163767 016572 010152 SUB @#B,TEMP
2072 006452 005767 010146 TST TEMP
2073 006456 001401 BEQ ,+4
2074 006460 104000 HLT
2075 006462 104400 SCOPE ;SUB FAILED
2076 :TEST ADD INDIRECT
2077 006464 005000 CLR %0
2078 006466 063700 016572 ADD @#B,%0
2079 006472 022700 125252 CMP #125252,%0
2080 006476 001401 BEQ ,+4
2081 006500 104000 HLT
2082 006502 104400 SCOPE ;ADD FAILED
2083
2084 006504 005037 016624 CLR @#TEMP
2085 006510 062737 125252 016624 ADD #125252,@#TEMP
2086 006516 022737 125252 016624 CMP #125252,@#TEMP
2087 006524 001401 REQ ,+4
2088 006526 104000 HLT
2089 006530 104400 SCOPE ;CLR OR ADD FAILED
2090 006532 012737 125252 016624 MOV #125252,@#TEMP
2091 006540 067737 010044 016624 ADD @A+6,@#TEMP
2092 006546 023727 016624 177777 CMP @#TEMP,-#1
2093 006554 001401 BEQ ,+4
2094 006556 104000 HLT
2095 006560 104400 SCOPE ;ADD FAILED
2096 :TEST UNARYS INDIRECT
2097 006562 012737 177777 016624 MOV #-1,@#TEMP
2098 006570 005037 016624 CLR @#TEMP
2099 006574 005737 016624 TST @#TEMP
2100 006600 001401 BEQ ,+4
2101 006602 104000 HLT
2102 006604 104400 SCOPE ;TST FAILED
2103
2104 006606 012737 125252 016624 MOV #125252,@#TEMP
2105 006614 005137 016624 COM @#TEMP
2106 006620 022737 052525 016624 CMP #052525,@#TEMP
2107 006626 001401 BEQ ,+4
2108 006630 104000 HLT
2109 006632 104400 SCOPE ;COM FAILED
2110
2111 006634 005037 016624 CLR @#TEMP
2112 006640 005237 016624 INC @#TEMP
2113 006644 022737 000001 016624 CMP #1,@#TEMP
2114 006652 001401 BEQ ,+4
2115 006654 104000 HLT
2116 006656 104400 SCOPE ;INC FAILED

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2117
2118 006660 005037 016624 CLR @#TEMP
2119 006664 005377 007736 DEC @TEMP+2
2120 006670 023727 016624 177777 CMP @#TEMP, #-1
2121 006676 001401 BEQ .+4
2122 006700 104000 HLT ;DEC FAILED
2123 006702 104400 SCOPE
2124
2125 006704 012737 000001 016624 MOV #1,@#TEMP
2126 006712 005437 016624 NEG @#TEMP
2127 006716 022737 177777 016624 CMP #-1,@#TEMP
2128 006724 001401 BEQ .+4
2129 006726 104000 HLT ;NEG FAILED
2130 006730 104400 SCOPE
2131
2132 :TEST INDIRECT ADDRESSING WITH INDEXING
2133 :TEST COMPARE INSTRUCTION
2134 006732 027727 007636 125252 CMP @B+2,#125252
2135 006740 001401 BEQ .+4
2136 006742 104000 HLT ;CMP FAILED
2137 006744 104400 SCOPE
2138
2139 006746 022777 125252 007620 CMP #125252,@B+2
2140 006754 001401 BEQ .+4
2141 006756 104000 HLT ;CMP FAILED
2142 006760 104400 SCOPE
2143
2144 006762 027777 007606 007604 CMP @B+2,@B+2
2145 006770 001401 BEQ .+4
2146 006772 104000 HLT ;CMP FAILED
2147 006774 104400 SCOPE
2148
2149 :TEST MOVE INSTRUCTIONS
2150 006776 017700 007572 MOV @B+2,%0
2151 007002 022700 125252 CMP #125252,%0
2152 007006 001401 BEQ .+4
2153 007010 104000 HLT ;MOV FAILED
2154 007012 104400 SCOPE
2155
2156 007014 012777 125252 007604 MOV #125252,@TEMP+2
2157 007022 023737 016572 016624 CMP @#B,@#TEMP
2158 007030 001401 BEQ .+4
2159 007032 104000 HLT ;MOV FAILED
2160 007034 104400 SCOPE
2161
2162 007036 017777 007532 007552 MOV @B+2,%C+2
2163 007044 023737 016572 016614 CMP @#B,@#C
2164 007052 001401 BEQ .+4
2165 007054 104000 HLT
2166 007056 104400 SCOPE
2167
2168 :TEST BIC INSTRUCTION INDIRECT WITH INDEXING
2169 007060 012700 177777 MOV #-1,%0
2170 007064 047700 007504 BIC @B+2,%0

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2171 007070 020027 052525 CMP %0,#52525
2172 007074 001401 BEQ .+4
2173 007076 104000 HLT ;BIC FAILED
2174 007100 104400 SCOPE
2175
2176 007102 012737 177777 016624 MOV #-1,@#TEMP
2177 007110 042777 125252 007510 BIC #125252,@TEMP+2
2178 007116 022737 052525 016624 CMP #52525,@#TEMP
2179 007124 001401 BEQ .+4
2180 007126 104000 HLT ;BIC FAILED
2181 007130 104400 SCOPE
2182
2183 007132 012737 177777 016614 MOV #-1,@#C
2184 007140 047777 007430 007450 BIC @B+2,@C+2
2185 007146 026737 007440 016614 CMP A+10,@#C
2186 007154 001401 BEQ .+4
2187 007156 104000 HLT ;BIC FAILED
2188 007160 104400 SCOPE
2189
2190 007162 012700 125252 MOV #125252,%0
2191 007166 167730 007402 SUB @B+2,%0
2192 007172 020027 000000 CMP %0,#0
2193 007176 001401 BEQ .+4
2194 007200 104000 HLT ;SUB FAILED
2195 007202 104400 SCOPE
2196
2197 007204 012737 125252 016624 MOV #125252,@#TEMP
2198 007212 166777 007354 007406 SUB B,@TEMP+2
2199 007220 001401 REQ .+4
2200 007222 104000 HLT ;SUB FAILED
2201 007224 104400 SCOPE
2202
2203 007226 012737 125252 016624 MOV #125252,@#TEMP
2204 007234 167777 007334 007364 SUB @B+2,@TEMP+2
2205 007242 005737 016624 TST @#TEMP
2206 007246 001401 BEQ .+4
2207 007250 104000 HLT ;SUB FAILED
2208 007252 104400 SCOPE
2209
2210 ;TEST ADD INDIRECT WITH INDEXING
2211 007254 005000 CLR %0
2212 007256 067700 007312 ADD @B+2,%0
2213 007262 022700 125252 CMP #125252,%0
2214 007266 001401 BEQ .+4
2215 007270 104000 HLT ;ADD FAILED
2216 007272 104400 SCOPE
2217
2218 007274 005037 016624 CLR @#TEMP
2219 007300 062777 125252 007320 ADD #125252,@TEMP+2
2220 007306 022737 125252 016624 CMP #125252,@#TEMP
2221 007314 001401 BEQ .+4
2222 007316 104000 HLT ;ADD FAILED
2223 007320 104400 SCOPE
2224 007322 012737 125252 016624 MOV #125252,@#TEMP

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2225 007330 067777 007254 007270 ADD @A+6,@#TEMP+2
2226 007336 023727 016624 177777 CMP @#TEMP,#-1
2227 007344 001401 BEQ .+4
2228 007346 104000 HLT
2229 007350 104400 SCOPE ;ADD FAILED
2230
2231 007352 012737 177777 016624 ;TEST UNARYS INDIRECT WITH INDEXING
2232 007360 005077 007242 MOV #-1,@#TEMP
2233 007364 005737 016624 CLR @TEMP+2
2234 007370 001401 TST @#TEMP
2235 BEQ .+4
2236 007372 104000 HLT ;TST FAILED
2237 007374 104400 SCOPE
2238
2239 007376 012737 125252 016624 MOV #125252,@#TEMP
2240 007404 005177 007216 COM @TEMP+2
2241 007410 022737 052525 016624 CMP #052525,@#TEMP
2242 BEQ .+4
2243 007420 104000 HLT ;COM FAILED
2244 007422 104400 SCOPE
2245
2246 007424 005037 016624 CLR @#TEMP
2247 007430 005277 007172 INC @TEMP+2
2248 007434 022737 000021 016624 CMP #1,@#TEMP
2249 BEQ .+4
2250 007444 104000 HLT ;INC FAILED
2251 007446 104400 SCOPE
2252
2253 007450 005037 016624 CLR @#TEMP
2254 007454 005377 007146 DEC @TEMP+2
2255 007460 023727 016624 177777 CMP @#TEMP,#-1
2256 007466 001401 BEQ .+4
2257 007470 104000 HLT ;DEC FAILED
2258 007472 104400 SCOPE
2259
2260 007474 012737 000021 016624 MOV #1,@#TEMP
2261 007502 005477 007120 NEG @TEMP+2
2262 007506 022737 177777 016624 CMP #-1,@#TEMP
2263 BEQ .+4
2264 007516 104000 HLT ;NEG FAILED
2265 007520 104400 SCOPE
2266
2267 007522 012737 177777 016624 MOV #-1,@#TEMP
2268 007530 000261 SEC
2269 007532 005577 007070 ADC @TEMP+2
2270 007536 005737 016624 TST @#TEMP
2271 007542 001401 BEQ .+4
2272 007544 104000 HLT ;ADC FAILED
2273 007546 104400 SCOPE
2274
2275 007550 012737 000021 016624 MOV #1,@#TEMP
2276 007556 000261 SEC
2277 007560 005677 007042 SBC @TEMP+2
2278 007564 005737 016624 TST @#TEMP

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2279 007570 001401 REQ .+4
2280 007572 104000 HLT ;ISBC FAILED
2281 007574 104400 SCOPE
2282
2283 ;TEST OF COMBINED INDEXING AND INDIRECT
2284 007576 012700 177772 MOV #-6,%0
2285 007602 027027 016602 125252 CMP @A(0),#125252
2286 007610 001401 BEQ .+4
2287 007612 104000 HLT ;CMP FAILED
2288 007614 104400 SCOPE
2289
2290 007616 012700 177772 MOV #-6,%0
2291 007622 022770 125252 016602 CMP #125252,@A(0)
2292 007630 001401 BEQ .+4
2293 007632 104000 HLT ;CMP FAILED
2294 007634 104400 SCOPE
2295
2296 007636 012700 177772 MOV #-6,%0
2297 007642 012701 000002 MOV #+2,%1
2298 007646 027071 016602 016602 CMP @A(0),@A(1)
2299 007654 001401 BEQ .+4
2300 007656 104000 HLT ;CMP FAILED
2301 007660 104400 SCOPE
2302
2303 ;TEST BIC INSTRUCTION
2304 007662 012700 000006 MOV #+6,%0
2305 007666 012767 177777 006730 MOV #-1,TEMP
2306 007674 047067 016602 006722 BIC @A(0),TEMP
2307 007702 022767 125252 006714 CMP #125252,TEMP
2308 007710 001401 BEQ .+4
2309 007712 104000 HLT ;BIC FAILED
2310 007714 104400 SCOPE
2311
2312 007716 012700 177772 MOV #-6,%0
2313 007722 012737 177777 016614 MOV #-1,@#C
2314 007730 042770 125252 016624 BIC #125252,@TEMP(0)
2315 007736 023727 016614 052525 CMP @#C,#052525
2316 007744 001401 BEQ .+4
2317 007746 104000 HLT ;BIC FAILED
2318 007750 104400 SCOPE
2319 007752 012737 177777 016614 MOV #-1,@#C

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2320 007760 012700 177772 MOV #-6,%0
2321 007764 012701 177772 MOV #-6,%1
2322 007770 047071 016602 016624 RIC @A(0),@TEMP(1)
2323 007776 022737 052525 016614 CMP #052525,%C
2324 010004 001401 BEQ .+4
2325 010006 104000 HLT ;BIC FAILED
2326 010010 104400 SCOPE
2327
2328 010012 122727 000000 000001 CMPB #0,%1 ;T7 FIX
2329 010020 002401 BLT .+4
2330 010022 104000 HLT ;CMPB FAILED
2331 010024 104400 SCOPE
2332 :TEST COMPARE INSTRUCTION INDEXED
2333 010026 012700 177770 MOV #-10,%0 ;MINUS 10 TO REG 0
2334 010032 126027 016602 000252 CMPB A(0),#000252 ;(A INDEX BY MINUS 10) TO #125252
2335 010040 001401 BEQ .+4
2336 010042 104000 HLT ;COMPARE WITH INDEX FAILED
2337 010044 104400 SCOPE
2338
2339 010046 012700 177770 MOV #-10,%0 ;FOR INDEX
2340 010052 122760 000252 016602 CMPB #000252,A(0) ;A INDEXED
2341 010060 001401 BEQ .+4
2342 010062 104000 HLT ;CMPB FAILED
2343 010064 104400 SCOPE
2344
2345 010066 012700 000010 MOV #10,%0 ;INDEX
2346 010072 126027 016602 000125 CMPB A(0),#000125
2347 010100 001401 BEQ .+4
2348 010102 104000 HLT ;CMPB FAILED
2349 010104 104400 SCOPE
2350
2351 010106 012700 000010 MOV #10,%0
2352 010112 122760 000125 016602 CMPB #000125,A(0)
2353 010120 001401 BEQ .+4
2354 010122 104000 HLT ;CMPB FAILED
2355 010124 104400 SCOPE
2356
2357 010126 012700 177770 MOV #-12,%0
2358 010132 126060 016602 016602 CMPB A(0),A(0)
2359 010140 001401 BEQ .+4
2360 010142 104000 HLT ;CMPB FAILED
2361 010144 104400 SCOPE
2362
2363 010146 012700 000010 MOV #+12,%0
2364 010152 126060 016602 016602 CMPB A(0),A(0)
2365 010160 001401 BEQ .+4
2366 010162 104000 HLT ;CMPB FAILED
2367 010164 104400 SCOPE
2368
2369 010166 012700 177770 MOV #-12,%0
2370 010172 012701 000004 MOV #+4,%1
2371 010176 126061 016602 016602 CMPB A(0),A(1)
2372 010204 001401 BEQ .+4
2373 010206 104000 HLT ;CMPB FAILED

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2374 010210 104400 SCOPE
2375
2376 010212 126160 316602 016602 CMPB A(1),A(0)
2377 010220 001401 SEQ .+4
2378 010222 104000 HLT ;CMPB FAILED
2379 010224 104400 SCOPE
2380
2381 010226 012700 177774 MOV #-4,%0
2382 010232 012701 000010 MOV #+10,%1
2383 010236 126061 016602 016602 CMPB A(0),A(1)
2384 010244 001401 REQ .+4
2385 010246 104000 HLT ;CMPB FAILED
2386 010250 104400 SCOPE
2387
2388 010252 012700 177774 MOV #-4,%0
2389 010256 012701 000010 MOV #10,%1
2390 010262 126160 016602 016602 CMPB A(1),A(0)
2391 010270 001401 REQ .+4
2392 010272 104000 HLT ;CMPB FAILED
2393 010274 104400 SCOPE
2394 :TEST MOVE INSTRUCTION FOR INDEX
2395
2396 010276 012700 177770 MOV #-10,%0
2397 010302 116067 016602 006314 MOVB A(0),TEMP
2398 010310 126727 006310 000252 CMPB TEMP,#000252
2399 010316 001401 REQ .+4
2400 010320 104000 HLT ;MOVE FAILED
2401 010322 104400 SCOPE
2402
2403 010324 012700 000010 MOV #+10,%0
2404 010330 116067 016602 006266 MOVB A(0),TEMP
2405 010336 126727 006262 000125 CMPB TEMP,#000125
2406 010344 001401 REQ .+4
2407 010346 104000 HLT ;MOVE FAILED
2408 010350 104400 SCOPE
2409
2410 010352 012700 177770 MOV #-10,%0
2411 010356 112760 125252 016624 MOVB #125252,TEMP(0)
2412 010364 123727 016614 125252 CMPB @#C,#125252
2413 010372 001401 REQ .+4
2414 010374 104000 HLT ;MOVB FAILED
2415 010376 104400 SCOPE
2416
2417 010400 012700 000010 MOV #+10,%0
2418 010404 112760 052525 016624 MOVB #052525,TEMP(0)
2419 010412 123727 016634 052525 CMPB @#TEMP+10,#052525
2420 010420 001401 REQ .+4
2421 010422 104000 HLT ;MOVB FAILED
2422 010424 104400 SCOPE
2423
2424 :TEST BIC INSTRUCTION FOR INDEXING
2425 010426 012767 177777 006170 MOV #-1,TEMP
2426 010434 012700 177770 MOV #-10,%0
2427 010440 146067 016672 006156 BICB A(0),TEMP

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2428 010446 126727 006132 177525 CMPB TEMP,#177525
2429 010454 001401 BEQ .+4 ;BICB FAILED
2430 010456 104000 HLT
2431 010460 104400 SCOPE
2432
2433 010462 012767 177777 006134 MOV #-1,TEMP
2434 010470 012700 000010 MOV #10,%0
2435 010474 146067 016602 006122 RICB A(0),TEMP
2436 010502 126727 006116 007652 CMPB TEMP,#007652
2437 010510 001401 BEQ .+4
2438 010512 104000 HLT ;BICB FAILED
2439 010514 104400 SCOPE
2440
2441 010516 012737 177777 016634 MOV #-1,@#TEMP+10
2442 010524 012700 000010 MOV #10,%0
2443 010530 142760 125252 016624 BICB #125252,TEMP(0)
2444 010536 123727 016634 002525 CMPB @#TEMP+10,#2525
2445 010544 001401 BEQ .+4
2446 010546 104000 HLT ;BICB FAILED
2447 010550 104400 SCOPE
2448
2449 010552 012700 177770 MOV #-10,%0
2450 010556 012767 177777 006030 MOV #-1,TEMP-10
2451 010564 142767 052525 006022 BICB #052525,TEMP-10
2452 010572 126727 006016 125252 CMPB TEMP-10,#125252
2453 010600 001401 BEQ .+4
2454 010602 104000 HLT ;BICB FAILED
2455 010604 104400 SCOPE
2456
2457 ;TEST UNARYS INDEXED
2458 010606 012737 177777 016624 MOV #-1,@#TEMP
2459 010614 012700 177770 MOV #-10,%0
2460 010620 105060 016634 CLRB D(0)
2461 010624 105737 016624 TSTB @#TEMP
2462 010630 001401 BEQ .+4
2463 010632 104000 HLT ;CLRB FAILED
2464 010634 104400 SCOPE
2465
2466 010636 012737 177777 016624 MOV #-1,@#TEMP
2467 010644 012700 177770 MOV #-10,%0
2468 010650 105060 016634 CLRB D(0)
2469 010654 023727 016624 177400 CMP @#TEMP,#177400
2470 010662 001401 BEQ .+4
2471 010664 104000 HLT ;CLRB FAILED
2472 010666 104400 SCOPE
2473
2474 010670 012737 177777 016624 MOV #-1,@#TEMP
2475 010676 012700 177771 MOV #-7,%0
2476 010702 105060 016634 CLRB D(0)
2477 010706 023727 016624 000377 CMP @#TEMP,#000377
2478 010714 001401 BEQ .+4
2479 010716 104000 HLT ;CLRB FAILED
2480 010720 104400 SCOPE
2481

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2482 010722 012737 177777 016624 MOV #-1,@#TEMP
2483 010730 012700 000010 MOV #+10,%0
2484 010734 105060 016614 CLRB C(0)
2485 010740 105737 016624 TSTB @#TEMP
2486 010744 001401 BEQ .+4
2487 010746 104000 HLT
2488 010750 104400 SCOPE ;CLRB FAILED
2489
2490 010752 012737 177777 016624 MOV #-1,@#TEMP
2491 010760 012700 177770 MOV #-12,%0
2492 010764 105160 016634 COMB D(0)
2493 010770 105737 016624 TSTB @#TEMP
2494 010774 001401 BEQ .+4
2495 010776 104000 HLT ;COMB FAILED
2496 011000 104400 SCOPE
2497
2498 011002 012737 177777 016624 MOV #-1,@#TEMP
2499 011010 012700 000010 MOV #10,%0
2500 011014 105160 016614 COMB C(0)
2501 011020 105737 016624 TSTB @#TEMP
2502 011024 001401 BEQ .+4
2503 011026 104000 HLT ;COMB FAILED
2504 011030 104400 SCOPE
2505 011032 012737 177777 016624 MOV #-1,@#TEMP
2506 011040 012700 177770 MOV #-10,%0
2507 011044 105260 016634 INCB D(0)
2508 011050 105737 016624 TSTB @#TEMP
2509 011054 001401 BEQ .+4
2510 011056 104000 HLT ;INCB FAILED
2511 011060 023727 016624 177400 CMP @#TEMP,#177400
2512 011066 001401 BEQ .+4
2513 011070 104000 HLT ;INCB FAILED
2514 011072 104400 SCOPE
2515
2516 011074 012737 177777 016624 MOV #-1,@#TEMP
2517 011102 012700 000010 MOV #+10,%0
2518 011106 105260 016614 INCB C(0)
2519 011112 105737 016624 TSTB @#TEMP
2520 011116 001401 BEQ .+4
2521 011120 104000 HLT ;INCB FAILED
2522 011122 104400 SCOPE
2523
2524 011124 012737 000001 016624 MOV #1,@#TEMP
2525 011132 012700 177770 MOV #-12,%0
2526 011136 105360 016634 DECB D(0)
2527 011142 105737 016624 TSTB @#TEMP
2528 011146 001401 BEQ .+4
2529 011150 104000 HLT ;DECB FAILED
2530 011152 104400 SCOPE
2531
2532 011154 012737 000001 016624 MOV #1,@#TEMP
2533 011162 012700 000010 MOV #10,%0
2534 011166 105360 016614 DECB C(0)
2535 011172 105737 016624 TSTB @#TEMP

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2536 011176 001401 SEQ .+4
2537 011200 104000 HLT ;DECB FAILED
2538 011202 104400 SCOPE
2539
2540 011204 012737 000001 016624 MOV #1,@#TEMP
2541 011212 012700 177770 MOV #-10,%0
2542 011216 105460 016634 NEGB D(0)
2543 011222 023727 016624 000377 CMP @#TEMP,#377
2544 011230 001401 BEQ .+4
2545 011232 104000 HLT ;NEGB FAILED
2546 011234 104400 SCOPE
2547
2548 011236 012737 000001 016624 MOV #1,@#TEMP
2549 011244 012700 000010 MOV #+10,%0
2550 011250 105460 016614 NEGB C(0)
2551 011254 023727 016624 000377 CMP @#TEMP,#377
2552 011262 001401 BEQ .+4
2553 011264 104000 HLT ;NEGB FAILED
2554 011266 104400 SCOPE
2555
2556 011270 012737 177777 016624 MOV #-1,@#TEMP
2557 011276 012700 177770 MOV #-10,%0
2558 011302 000261 SEC
2559 011304 105560 016634 ADCB D(0)
2560 011310 023727 016624 177400 CMP @#TEMP,#177400
2561 011316 001401 BEQ .+4
2562 011320 104000 HLT ;ADCB FAILED
2563 011322 104400 SCOPE
2564
2565 011324 012737 177777 016624 MOV #-1,@#TEMP
2566 011332 012700 000010 MOV #+10,%0
2567 011336 000261 SEC
2568 011340 105560 016614 ADCB C(0)
2569 011344 023727 016624 177400 CMP @#TEMP,#177400
2570 011352 001401 BEQ .+4
2571 011354 104000 HLT ;ADCB FAILED
2572 011356 104400 SCOPE
2573
2574 011360 012737 000401 016624 MOV #401,@#TEMP
2575 011366 012700 177771 MOV #-7,%0
2576 011372 000261 SEC
2577 011374 105660 016634 SBCB D(0)
2578 011400 022737 000001 016624 CMP #1,@#TEMP
2579 011406 001401 BEQ .+4
2580 011410 104000 HLT ;SBCB FAILED
2581 011412 104400 SCOPE
2582
2583 011414 012737 000001 016624 MOV #1,@#TEMP
2584 011422 012700 000010 MOV #+10,%0
2585 011426 000261 SEC
2586 011430 105660 016614 SBCB C(0)
2587 011434 005737 016624 TST @#TEMP
2588 011440 001401 BEQ .+4
2589 011442 104000 HLT ;SBCB FAILED

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2590 011444 104400 SCOPE
2591
2592 ; TEST INDIRECT ADDRESSING
2593 ; TEST COMPARE INSTRUCTION
2594 011446 123727 016572 000252 CMPB @#B,#000252
2595 011454 001401 BEQ .+4
2596 011456 104000 HLT ; CMPB FAILED
2597 011460 104400 SCOPE
2598
2599 011462 123727 016573 000252 CMPB @#B+1,#252
2600 011470 001401 BEQ .+4
2601 011472 104000 HLT ; CMPB FAILED
2602 011474 104400 SCOPE
2603
2604
2605 011476 122737 125252 016572 CMPB #125252,@#B
2606 011504 001401 BEQ .+4
2607 011506 104000 HLT ; CMPB FAILED
2608 011510 104400 SCOPE
2609
2610 011512 123737 016572 016572 CMPB @#B,@#B
2611 011520 001401 BEQ .+4
2612 011522 104000 HLT ; CMPB FAILED
2613 011524 104400 SCOPE
2614
2615 ; TEST MOVE INSTRUCTIONS
2616 011526 113700 016572 MOVB @#B,%0
2617 011532 122700 000252 CMPB #000252,%0
2618 011536 001401 BEQ .+4
2619 011540 104000 HLT ; MOVB FAILED
2620 011542 104400 SCOPE
2621
2622 011544 112737 125252 016624 MOVB #125252,@#TEMP
2623 011552 126737 005014 016624 CMPB B,@#TEMP
2624 011560 001401 BEQ .+4
2625 011562 104000 HLT ; MOVB FAILED
2626 011564 104400 SCOPE
2627
2628 011566 113737 016572 016614 MOVB @#B,@#C
2629 011574 126737 004772 016614 CMPB B,@#C
2630 011602 001401 BEQ .+4
2631 011604 104000 HLT ; MOVB FAILED
2632 011606 104400 SCOPE
2633 ; TEST UNARYS INDIRECT
2634 011610 012737 177777 016624 MOV #-1,@#TEMP
2635 011616 105037 016624 CLR B @#TEMP
2636 011622 023727 016624 177400 CMP @#TEMP,#177400
2637 011630 001401 BEQ .+4
2638 011632 104000 HLT ; CLR B FAILED
2639 011634 104400 SCOPE
2640
2641 011636 012737 125252 016624 MOV #125252,@#TEMP
2642 011644 105137 016624 COMB @#TEMP
2643 011650 022737 125125 016624 CMP #125125,@#TEMP

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2644 011656 001401 BEQ ,+4
2645 011660 104000 HLT ;COMB FAILED
2646 011662 104400 SCOPE
2647
2648 011664 012737 125252 016624 MOV #125252,%#TEMP
2649 011672 105137 016625 COMB %#TEMP+1
2650 011676 022737 052652 016624 CMP #052652,%#TEMP
2651 011704 001401 BEQ ,+4
2652 011706 104000 HLT ;COMB FAILED
2653 011710 104400 SCOPE
2654
2655 011712 005037 016624 CLR %#TEMP
2656 011716 105237 016625 INCB %#TEMP+1
2657 011722 022737 000400 016624 CMP #402,%#TEMP
2658 011730 001401 BEQ ,+4
2659 011732 104000 HLT ;INCB FAILED
2660 011734 104400 SCOPE
2661
2662 011736 005037 016624 CLR %#TEMP
2663 011742 105377 004650 DECB %#TEMP+2
2664 011746 023727 016624 000377 CMP %#TEMP,#377
2665 011754 001401 BEQ ,+4
2666 011756 104000 HLT ;DECB FAILED
2667 011762 104400 SCOPE
2668
2669 011762 005037 016624 CLR %#TEMP
2670 011766 112737 000001 016625 MOVB #1,%#TEMP+1
2671 011774 105437 016625 NEG B %#TEMP+1
2672 012000 022737 177400 016624 CMP #177400,%#TEMP
2673 012006 001401 BEQ ,+4
2674 012010 104000 HLT ;NEGR FAILED
2675 012012 104400 SCOPE
2676
2677 ;TEST INDIRECT ADDRESSING WITH INDEXING
2678 ;TEST COMPARE INSTRUCTION
2679 012014 127727 004554 125252 CMPB @B+2,#125252
2680 012022 001401 BEQ ,+4
2681 012024 104000 HLT ;CMPB FAILED
2682 012026 104400 SCOPE
2683
2684 012030 122777 125252 004536 CMPB #125252,%B+2
2685 012036 001401 BEQ ,+4
2686 012040 104000 HLT ;CMPB FAILED
2687 012042 104400 SCOPE
2688
2689 012044 127777 004524 004522 CMPB @B+2,%B+2
2690 012052 001401 BEQ ,+4
2691 012054 104000 HLT ;CMPB FAILED
2692 012056 104400 SCOPE
2693 ;TEST MOVE INSTRUCTIONS
2694 012060 117700 004510 MOVB @B+2,%0
2695 012064 122700 125252 CMPB #125252,%0
2696 012070 001401 BEQ ,+4
2697 012072 104000 HLT ;MOVB FAILED

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2698 012074 104400 SCOPE
2699
2700 012076 112777 125252 004522 MOVB #125252,@TEMP+2
2701 012104 126737 004452 016624 CMPB B,@#TEMP
2702 012112 001401 BEQ .+4
2703 012114 104000 HLT ;MOVB FAILED
2704 012116 104400 SCOPE
2705
2706 012120 117777 004450 004470 MOVB @B+2,@C+2
2707 012126 126737 004440 016614 CMPB B,@#C
2708 012134 001401 BEQ .+4
2709 012136 104000 HLT ;MOVR FAILED
2710 012140 104400 SCOPE
2711
2712 ;TEST BIC INSTRUCTION INDIRECT WITH INDEXING
2713 012142 012700 177777 MOV #-1,%0
2714 012146 147700 004422 BICB @B+2,%0
2715 012152 120027 052525 CMPB %0,#52525
2716 012156 001401 BEQ .+4
2717 012160 104000 HLT ;BICB FAILED
2718 012162 104400 SCOPE
2719
2720 012164 012737 177777 016624 MOV #-1,@#TEMP
2721 012172 142777 125252 004426 BICB #125252,@TEMP+2
2722 012200 122737 052525 016624 CMPB #52525,@#TEMP
2723 012206 001401 BEQ .+4
2724 012210 104000 HLT ;BICB FAILED
2725 012212 104400 SCOPE
2726
2727 012214 012737 177777 016614 MOV #-1,@#C
2728 012222 147777 004346 004366 BICB @B+2,@C+2
2729 012230 126737 004356 016614 CMPB A+12,@#C
2730 012236 001401 BEQ .+4
2731 012240 104000 HLT ;BICB FAILED
2732 012242 104400 SCOPE
2733 ;TEST UNARYS INDIRECT WITH INDEXING
2734 012244 012737 177777 016624 MOV #-1,@#TEMP
2735 012252 105077 004350 CLR B @TEMP+2
2736 012256 105737 016624 TSTB @#TEMP
2737 012262 001401 BEQ .+4
2738 012264 104000 HLT ;CLRR FAILED
2739 012266 104400 SCOPE
2740
2741 012270 012737 125252 016624 MOV #125252,@#TEMP
2742 012276 105177 004324 COMB @TEMP+2
2743 012302 122737 052525 016624 CMPB #052525,@#TEMP
2744 012310 001401 BEQ .+4
2745 012312 104000 HLT ;COMB FAILED
2746 012314 104400 SCOPE
2747
2748 012316 005037 016624 CLR @#TEMP
2749 012322 105277 004300 INC B @TEMP+2
2750 012326 122737 000001 016624 CMPB #1,@#TEMP
2751 012334 001401 BEQ .+4

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2752 012336 104000 HLT ;INCBL FAILED
2753 012340 104400 SCOPE
2754
2755 012342 005037 016624 CLR @#TEMP
2756 012346 105377 004254 DECB @TEMP+2
2757 012352 123727 016624 177777 CMPB @#TEMP, #-1
2758 012360 001401 BEQ .+4
2759 012362 104000 HLT ;DECBL FAILED
2760 012364 104400 SCOPE
2761
2762 012366 012737 000001 016624 MQV #1,@#TEMP
2763 012374 105477 004226 NEG B @TEMP+2
2764 012400 122737 177777 016624 CMPB #-1,@#TEMP
2765 012406 001401 BEQ .+4
2766 012410 104000 HLT ;NEGBL FAILED
2767 012412 104400 SCOPE
2768
2769 012414 012737 177777 016624 MOV #-1,@#TEMP
2770 012422 000261 SEC
2771 012424 105577 004176 ADCB @TEMP+2
2772 012430 022737 177400 016624 CMP #177400,@#TEMP
2773 012436 001401 BEQ .+4
2774 012440 104000 HLT ;ADCBL FAILED
2775 012442 105737 016624 TSTB @#TEMP
2776 012446 001401 BEQ .+4
2777 012450 104000 HLT ;TSTBL FAILED
2778 012452 104400 SCOPE
2779
2780 012454 012737 000001 016624 MOV #1,@#TEMP
2781 012462 000261 SEC
2782 012464 105377 004136 DECB @TEMP+2
2783 012470 005737 016624 TST @#TEMP
2784 012474 001401 BEQ .+4
2785 012476 104000 HLT ;DECBL FAILED
2786 012500 104400 SCOPE
2787
2788 :TEST OF COMBINED INDEXING AND INDIRECT
2789 012502 012700 177772 MOV #-6,%0
2790 012506 127027 016602 125252 CMPB @A(0),#125252
2791 012514 001401 BEQ .+4
2792 012516 104000 HLT ;CMPB FAILED
2793 012520 104400 SCOPE
2794
2795 012522 012700 177772 MOV #-6,%0
2796 012526 122770 125252 016602 CMPB #125252,@A(2)
2797 012534 001401 BEQ .+4
2798 012536 104000 HLT ;CMPB FAILED
2799 012540 104400 SCOPE
2800
2801 012542 012700 177772 MOV #-6,%0
2802 012546 012701 000002 MOV #+2,%1
2803 012552 127071 016602 016602 CMPB @A(0),@A(1)
2804 012560 001401 BEQ .+4
2805 012562 104000 HLT ;CMPB FAILED

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2806 012564 104400 SCOPE
2807 ;TEST BIC INSTRUCTION
2808 012566 012700 000026 MOV #+6,%0
2809 012572 012767 177777 004024 MOV #-1,TEMP
2810 012600 147067 016602 004016 BICB @A(0),TEMP
2811 012606 122767 125252 004010 CMPB #125252,TEMP
2812 012614 001401 BEQ .+4
2813 012616 104000 HLT ;BICB FAILED
2814 012620 104400 SCOPE
2815
2816 012622 012700 177772 MOV #-6,%0
2817 012626 012737 177777 016614 MOV #-1,@#C
2818 012634 142772 125252 016624 BICB #125252,@TEMP(0)
2819 012642 123727 016614 000125 CMPB @#C,#000125
2820 012650 001401 BEQ .+4
2821 012652 104000 HLT ;BICB FAILED
2822 012654 104400 SCOPE
2823
2824 012656 012700 016574 MOV #B+2,%0 ;ADDRESS OF ADDRESS OF B
2825 012662 023067 003704 CMP @((0)+,B
2826 012666 001401 REQ .+4
2827 012670 104000 HLT ;CMP FAILED
2828 012672 104400 SCOPE
2829
2830 012674 012700 016576 MOV #B+4,%0
2831 012700 025067 003656 CMP @-(2),B
2832 012704 001401 REQ .+4
2833 012706 104000 HLT ;CMP FAILED
2834 012710 104400 SCOPE
2835
2836 012712 012700 016576 MOV #B+4,%0
2837 012716 125067 003650 CMPB @-(2),B
2838 012722 001401 REQ .+4
2839 012724 104000 HLT ;CMPB FAILED
2840 012726 104400 SCOPE
2841
2842 012730 012700 016620 MOV #C+4,%0
2843 012734 012737 177777 016614 MOV #-1,@#C
2844 012742 105050 CLR B @-(2)
2845 012744 023727 016614 177400 CMP @#C,#177400
2846 012752 001401 BEQ .+4
2847 012754 104000 HLT ;CLRR FAILED
2848 012756 104400 SCOPE
2849 012760 012737 177777 016614 MOV #-1,@#C
2850 012766 012700 177772 MOV #-6,%0
2851 012772 012701 177772 MOV #-6,%1
2852 012776 147071 016602 016624 BICB @A(0),@TEMP(1)
2853 013004 022737 177525 016614 CMP #177525,@#C
2854 013012 001401 BEQ .+4
2855 013014 104000 HLT ;BICB FAILED
2856 013016 104400 SCOPE
2857 ;TEST THAT R0 IS NOT DESTROYED BY FALSE SELECTION
2858 013020 012700 052525 MOV #52525,%0 ;THIS IS CHECK LATER IN PROGRAM
2859 ;TEST JSR INSTRUCTION

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2860
2861 013024 004767 000002 JSR %7, TJSR2 ;PLACE PC ON STACK
2862 013030 000405 BR TJSR3 ;RETURN HERE ON RTS %7
2863 013032 121627 013030 TJSR2: CMPB %6,#TJSR1 ;CHECK FOR CORRECT PC ON STACK
2864 013036 001401 BEQ .+4
2865 013040 104000 HLT
2866 013042 000207 RTS %7 ;INCORRECT PC ON STACK
2867 013044 104400 TJSR3: SCOPE ;RETURN TO INST AFTER JSR
2868
2869 013046 000257 CCC
2870 013050 004717 JSR %7,%7 ;INSTRUCTION UNDER TEST
2871 013052 121627 013052 CMPB %6,#TJSR3+6 ;TEST THE STACK
2872 013056 001401 BEQ .+4
2873 013060 104000 HLT
2874 013062 005726 TST (6)+- ;PC OF JSR DID NOT GO TO STACK
2875 013064 104400 SCOPE ;REPOSITION THE STACK
2876 :TEST NESTED SUBROUTINES
2877
2878 013066 000257 CCC
2879 013070 004767 003342 JSR %7,SUBR6 ;CLEAR CONDITION CODES
2880 013074 100401 BMI .+4
2881 013076 104000 HLT
2882 013100 001401 BEQ .+4 ;JSR OR RTS FAILED
2883 013102 104000 HLT
2884 013104 102401 BVS .+4 ;JSR OR RTS FAILED
2885 013106 104000 HLT
2886 013110 103401 BCS .+4 ;JSR OR RTS FAILED
2887 013112 104000 HLT
2888 013114 104400 SCOPE ;JSR OR RTS FAILED
2889 :TEST ROTATE ODD BYTE
2890 013116 104400 SCOPE
2891 013120 000257 CCC ;CLEAR "C"
2892 013122 012767 123456 003474 MOV #123456,TEMP
2893 013130 106067 003471 RORB TEMP+1 ;ROTATE ODD BYTE
2894 013134 103401 BCS .+4
2895 013136 104000 HLT ;C NOT SET
2896 013140 102401 BVS .+4
2897 013142 104000 HLT ;V NOT SET
2898 013144 022767 051456 003452 CMP #051456,TEMP
2899 013152 001401 BEQ .+4 ;ROTATE FAILED
2900 013154 104000 HLT
2901 013156 104400 SCOPE
2902 013160 000277 SCC ;SET C
2903 013162 012767 123456 003434 MOV #123456,TEMP
2904 013170 106067 003431 RORB TEMP+1
2905 013174 103401 BCS .+4
2906 013176 104000 HLT ;C NOT SET
2907 013200 102001 BVC .+4
2908 013202 104000 HLT ;V NOT CLEARED
2909 013204 022767 151456 003412 CMP #151456,TEMP
2910 013212 001401 BEQ .+4 ;ROTATE FAILED
2911 013214 104000 HLT
2912 013216 104400 SCOPE
2913

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2914 013220 000257 CCC
2915 013222 012767 123456 003374 MOV #123456,TEMP
2916 013230 106167 003371 ROLB TEMP+1
2917 013234 103401 BCS .+4
2918 013236 104000 HLT ;C NOT SET
2919 013240 102401 BVS .+4
2920 013242 104000 HLT ;V NOT SET
2921 013244 022767 047036 003352 CMP #047056,TEMP
2922 013252 001401 BEQ .+4
2923 013254 104000 HLT ;ROTATE BYTE FAILED
2924 013256 104400 SCOPE
2925
2926 013250 000277 SCC ;SET C
2927 013262 012767 123456 003334 MOV #123456,TEMP
2928 013270 106167 003331 ROLB TEMP+1
2929 013274 103401 BCS .+4
2930 013276 104000 HLT ;C NOT SET
2931 013300 102401 BVS .+4
2932 013302 104000 HLT ;V NOT SET
2933 013304 022767 047436 003312 CMP #047456,TEMP
2934 013312 001401 BEQ .+4
2935 013314 104000 HLT ;ROTATE ODD BYTE FAILED
2936 013316 104400 SCOPE
2937
2938 013320 000257 CCC ;CLEAR C
2939 013322 012767 177777 003274 MOV #-1,TEMP
2940 013330 106267 003271 ASRB TEMP+1
2941 013334 103401 BCS .+4
2942 013336 104000 HLT ;C NOT SET
2943 013340 102201 BVC .+4
2944 013342 104000 HLT ;V NOT CLEARED
2945 013344 026727 003254 177777 CMP TEMP, #-1
2946 013352 001401 BEQ .+4
2947 013354 104000 HLT ;SHIFT FAILED
2948 013356 104400 SCOPE
2949
2950 013360 000277 SCC
2951 013362 012767 177777 003234 MOV #-1,TEMP
2952 013370 106367 003231 ASLB TEMP+1
2953 013374 103401 BCS .+4
2954 013376 104000 HLT ;C NOT SET
2955 013400 102201 BVC .+4
2956 013402 104000 HLT ;V NOT CLEARED
2957 013404 026727 003214 177377 CMP TEMP, #177377
2958 013412 001401 BEQ .+4
2959 013414 104000 HLT ;SHIFT BYTE FAILED
2960 013416 104400 SCOPE
2961 ;TEST COMBINATION OF N, C AND V
2962 ,MACR TNCV
2963 BPL .+12
2964 BCC .+20
2965 BVC .+30 ;Z=1
2966 HLT ;Z=C, BUT V=1
2967 BR .+24

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2968 BCC .+16 ;Z=0
2969 BVS .+20 ;Z=0, C=1
2970 HLT
2971 BR .+14 ;Z NOT EQUAL C, V=1
2972 BVS .+12 ;Z=1, C=0
2973 HLT ;Z NOT EQUAL C, V=1
2974 BR .+6
2975 BVC .+4 ;Z=0, C=0
2976 HLT ;Z=C, BUT V=1
2977 SCOPE
2978 .ENDM
2979 013420 005037 016400 CLR @#ICOUNT ;NO ITERATION
2980 ;TEST ALL COMBINATIONS OF NUMBERS WITH COMPARE INSTRUCTION
2981 013424 005002 COMPAR: CLR %2 ;INIT %2
2982 013426 005001 CLR %1 ;INIT %1
2983 013430 020201 CMP1: CMP %2,%1 ;ARE THE EQUAL
2984 013432 001401 BEQ .+4
2985 013434 104000 HLT
2986 013436 020227 177777 CMP %2,%-1 ;R0 AND R1 DID NOT COMPARE
2987 013442 001403 BEQ CMP2 ;AT UPPER LIMIT
2988 013444 005202 INC %2 ;YES EXIT
2989 013446 005201 INC %1 ;INCREMENT TO NEXT NUMBER
2990 013450 000767 BR CMP1
2991 013452 104400 CMP2: SCOPE
2992
2993 ;TEST ROTATING ALL NUMBERS
2994 013454 104400 SCOPE
2995 013456 012767 177777 000132 MOV #1,REFF ;INITIALIZE BASE NUMBER
2996 013464 005267 000126 TSROT: INC REFF ;INCREMENT NUMBER
2997 013470 004767 000012 JSR %7,ROTALL ;GO TO COMPARE ROUTINE
2998 013474 026727 000116 177777 CMP REFF,#-1 ;TEST ALL VALUES
2999 013502 001370 BNE TSRCT ;NO TEST THEM ALL
3000 013504 000446 BR TSRCT2A ;WE ARE DONE
3001
3002 013506 016767 000104 000104 ROTALL: MOV REFF,TEST
3003 013514 006067 000100 ROR TEST
3004 013520 006067 000074 ROR TEST
3005 013524 006067 000070 ROR TEST
3006 013530 006167 000054 ROL TEST
3007 013534 006167 000050 ROL TEST
3008 013540 006167 000054 ROL TEST
3009 013544 TNCV
3010 013544 100004 RPL .+12 ;Z=1
3011 013546 103007 BCC .+20 ;Z=1, C=1
3012 013550 102013 BVC .+30 ;Z=C, PUT V=1
3013 013552 104000 HLT
3014 013554 000411 BR .+24 ;Z=0
3015 013556 103006 BCC .+16 ;Z=0, C=1
3016 013560 102407 BVS .+20 ;Z NOT EQUAL C, V=1
3017 013562 104000 HLT
3018 013564 000405 BR .+14 ;Z=1, C=0
3019 013566 102404 BVS .+12 ;Z NOT EQUAL C, V=1
3020 013570 104000 HLT
3021 013572 000402 BR .+6

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3022	013574	102001	RVC	.+4	:Z=0, C=0
3023	013576	104000	HLT		;Z=C, BUT V=1
3024	013600	104400	SCOPE		
3025	013602	026767 000012 000006	CMP	TEST,REFF	
3026	013610	001401	REQ	.+4	
3027	013612	104000	HLT		;INITIAL NOT EQUAL TO FINAL
3028	013614	000207	RTS	%7	
3029	013616	000000	REFF:	0	;GOOD DATA
3030	013620	000000	TEST:	0	;BAD DATA
3031	013616		REF=REFF		
3032			;TEST ROTATING BYTE EVEN/ODD, ALL NUMBERS		
3033	013622	012767 177777 177766	TSRT2A:	MOV #1,REFF	
3034	013630	005267 177762	TSROT2:	INC REFF	
3035	013634	014767 000016	JSR	%7,ROTBE	
3036	013640	004767 000122	JSR	%7,ROTBO	
3037	013644	022767 177777 177744	CMP	#-1,FEFF	
3038	013652	001366	RNE	TSRCT2	
3039	013654	000505	RR	ROTEM1	
3040	013656	016767 177734 177734	ROTBE:	MOV REFF,TEST	
3041	013664	106067 177730	RORB	TEST	;ROTATE BYTE EVEN
3042	013670	106267 177724	RORB	TEST	
3043	013674	106067 177720	RORB	TEST	
3044	013700	106167 177714	ROLB	TEST	
3045	013704	106167 177710	ROLB	TEST	
3046	013710	106167 177704	ROLB	TEST	
3047	013714		TNCV		
3048	013714	100004	BPL	.+12	
3049	013716	103007	BCC	.+20	:Z=1
3050	013720	102013	RVC	.+32	:Z=1, C=1
3051	013722	104000	HLT		;Z=C, BUT V=1
3052	013724	000411	RR	.+24	
3053	013726	103006	RCC	.+16	:Z=0
3054	013730	102407	RVS	.+22	:Z=0, C=1
3055	013732	104000	HLT		;Z NOT EQUAL C, V=1
3056	013734	000405	RR	.+14	
3057	013736	102404	BVS	.+12	:Z=1, C=0
3058	013740	104000	HLT		;Z NOT EQUAL C, V=1
3059	013742	000402	RR	.+6	
3060	013744	102001	RVC	.+4	:Z=0, C=0
3061	013746	104000	HLT		;Z=C, BUT V=1
3062	013750	104400	SCOPE		
3063	013752	026767 177642 177636	CMP	TEST,REFF	
3064	013760	001401	REQ	.+4	
3065	013762	104000	HLT		
3066	013764	000207	RTS	%7	
3067	013766	106067 177627	ROTBO:	RORB TEST+1	;ROTATE BYTE ODD
3068	013772	106067 177623	RORB	TEST+1	
3069	013776	106067 177617	RORB	TEST+1	
3070	014002	106167 177613	ROLB	TEST+1	
3071	014006	106167 177607	ROLB	TEST+1	
3072	014012	106167 177603	ROLB	TEST+1	
3073	014016		TNCV		
3074	014016	100004	BPL	.+12	
3075	014020	103007	BCC	.+20	:Z=1

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3076 014022 102013 BVC .+30 ;Z=1, C=1
3077 014024 104000 HLT ;Z=C, BUT V=1
3078 014026 000411 BR .+24
3079 014030 103006 RCC .+16 ;Z=0
3080 014032 102407 BVS .+20 ;Z=0, C=1
3081 014034 104000 HLT ;Z NOT EQUAL C, V=1
3082 014036 000405 BR .+14
3083 014040 102404 BVS .+12 ;Z=1, C=0
3084 014042 104000 HLT ;Z NOT EQUAL C, V=1
3085 014044 000402 BR .+6
3086 014046 102001 BVC .+4 ;Z=0, C=0
3087 014050 104000 HLT ;Z=C, BUT V=1
3088 014052 104400 SCOPE
3089 014054 026767 177540 177534 CMP TEST,REFF
3090 014062 001401 BEQ .+4
3091 014064 104000 HLT
3092 014066 000207 RTS %7
3093 014070 104400 ROTEN1: SCOPE
3094 ;ADD AND SUBTRACT ALL NUMBERS AGAINST FIXED NUMBERS
3095 ;A+B=C, C-A=B, BF SHOULD EQUAL BI
3096 014072 011667 000072 TSTAR1: MOV @%6,NUMA
3097 014076 012767 000001 177512 MCV #1,REF
3098 014104 005267 177506 ARITST: INC REF
3099 014110 004767 000014 JSR %7,ANSUB
3100 014114 022767 177777 177474 CMP #-1,REFF
3101 014122 001370 BNE ARITST
3102 014124 000422 BR ARIEND
3103 014126 104400 SCOPE
3104 014130 016767 177462 177462 ADSUB: MOV REF,TEST
3105 014136 066767 000026 177454 ADD NUMA,TEST
3106 014144 166767 000020 177446 SUB NUMA,TEST
3107 014152 026767 177440 177440 CMP REF,TEST
3108 014160 001401 BEQ .+4
3109 014162 104000 HLT
3110 014164 104400 SCOPE
3111 014166 000207 RTS %7
3112 014170 000000 NUMA 0
3113 014172 104400 ARIEND: SCOPE
3114 ;TEST COMPLIMENTING ALL NUMBERS
3115 014174 005067 002424 CLR TEMP ;BASE DATA
3116 014200 005067 002424 CLR TEMP+4 ;BASE REFERENCE
3118 014204 005167 002414 TCOMI COM TEMP ;COMPLIMENT DATA
3119 014210 005367 002414 DEC TEMP+4 ;DECREMENT REFERENCE
3120 014214 026767 002404 002406 CMP TEMP,TEMP+4 ;COMPARE
3121 014222 001401 BEQ .+4 ;TEST
3122 014224 104000 HLT ;COMPLIMENT OR DECREMENT FAILED
3123 014226 005167 002372 COM TEMP
3124 014232 005267 002366 INC TEMP ;INCREMENT AND TEST FOR DONE
3125 014236 001362 BNE TCOM ;NOT FINISHED GO LOOP
3126 014240 104400 SCOPE
3127 ;TEST COMB (EVEN BYTE)
3128 014242 005067 002356 CLR TEMP ;BASE DATA

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3130 014246 005067 002356 CLR TEMP+4 ;REFERENCE DATA
3131 014252 105167 002346 TCOM2: COMB TEMP
3132 014256 005367 002346 DEC TEMP+4
3133 014262 126767 002336 002340 CMPB TEMP,TEMP+4 ;COMPARE
3134 014270 001421 BEQ .+4
3135 014272 104000 HLT ;COMPLIMENT OR INCREMENT BYTE FAILED
3136 014274 105167 002324 COMB TEMP
3137 014300 105267 002320 INCB TEMP
3138 014304 001362 BNE TCOM2
3139 014306 104400 SCOPE
3140 ;TEST COMB (ODD BYTE)
3141 014310 005067 002310 CLR TEMP ;BASE DATA
3142 014314 005067 002310 CLR TEMP+4 ;REFERENCE DATA
3143 014320 105167 002301 TCOM3: COMB TEMP+1 ;ODD BYTE
3144 014324 005367 002300 DEC TEMP+4
3145 014330 126767 002271 002272 CMPB TEMP+1,TEMP+4
3146 014336 001401 BEQ .+4
3147 014340 104000 HLT ;COMPLIMENT BYTE FAILED
3148 014342 105167 002257 COMB TEMP+1
3149 014346 105267 002253 INCB TEMP+1
3150 014352 001362 BNE TCOM3
3151 014354 104400 SCOPE
3152
3153 ;TEST COMPARE ALL VALUE EVEN BYTE WITH ODD
3154 014356 005067 002242 CLR TEMP ;BASE VALUE
3155 014362 126767 002236 002235 TSCOMB: CMPB TEMP,TEMP+1 ;COMPARE
3156 014370 001401 BEQ .+4
3157 014372 104000 HLT ;COMPARE FAILED
3158 014374 0022001 BGE .+4
3159 014376 104000 HLT ;IV IS NOT = TO N
3160 014400 003401 BLE .+4
3161 014402 104000 HLT ;IV IS SET
3162 014404 062767 000401 002212 ADD #401,TEMP
3163 014412 022767 177777 002204 CMP #-1,TEMP
3164 014420 001360 BNE TSCOMB
3165 014422 104400 SCOPE
3166 014424 012737 004000 016400 MOV #4000,@#ICOUNT
3167 014432 104400 WAIT3: SCOPE
3168 014434 005767 002062 TST SAVR6 ;SET ON POWER FAIL
3169 014440 001405 BEQ WAITS ;SKIP OVER IF CLEAR
3170 014442 005067 002054 CLR SAVR6
3171 014446 104000 HLT ;POWER FAIL OCCURRED
3172 014450 000137 0000510 JMP @#ESTART
3173 014454 012737 000010 016400 WAIT5:
3174 014454 012737 000010 016400 MOV #10,@#ICOUNT
3175
3176 ;TEST TO SEE IF I/O DEVICES WERE SELECTED
3177 014462 123727 001362 000377 CMPB @#REG1,#377 ;SELECTED DEVICES STORED IN REG1
3178 014470 001404 BEQ WAIT4 ;BRANCH IF NO DEVICES SELECTED
3179 014472 000001 WAIT ;INTERRUPTS WILL OCCUR
3180 014474 000001 WAIT ;IF DEVICES ARE SELECTED
3181 014476 000001 WAIT
3182 014500 000001 WAIT
3183 014502 104400 WAIT4: SCOPE

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3184 014504 012737 004000 016400 MOV #4000, #ICOUNT
3185
3186 :TEST SWAB
3187 014512 012767 000200 177100 MOV #0200, TEST
3188 014520 000367 177074 SWAB TEST
3189 014524 100001 RPL .+4
3190 014526 104000 HLT
3191 014530 001401 BEQ .+4
3192 014532 104000 HLT
3193 014534 000367 177060 SWAB TEST
3194 014540 100401 BMI .+4
3195 014542 104000 HLT
3196 014544 001001 BNE .+4
3197 014546 104000 HLT
3198 014550 104400 SCOPE
3199 014552 005037 016400 CLR @#ICOUNT
3200
3201 :TEST ALL COMBINATIONS OF SWAB
3202 014556 005067 177036 CLR TEST JNUMBER UNDER TEST
3203 014562 005067 177030 CLR REF JREFERENCE NUMBER
3204 014566 000367 177026 SWABA: SWAB TEST JOPERATION UNDER TEST
3205 014572 026767 177022 177016 CMP TEST, REF JTEST SWAB INSTRUCTION
3206 014600 001401 BEQ .+4
3207 014602 104000 HLT JSWAB FAILED
3208 014604 000367 177010 SWAB TEST
3209 014610 005267 177002 INC REF JINCREMENT REFERENCE NUMBER
3210 014614 105267 177001 INCB TEST+1 JINC TEST NUMBER
3211 014620 001362 BNE SWABA JLOOP TILL DONE
3212 014622 104400 SCOPE
3213 014624 012737 004000 016400 MOV #4000, #ICOUNT
3214 000240 NOP=240
3215 177776 CC=177776
3216
3217 014632 012767 177777 001764 MOV #-1, TEMP
3218 014640 000261 SEC
3219 014642 105567 001757 ADCB TEMP+1
3220 014646 103401 BCS .+4
3221 014650 104000 HLT JADCB FAILED
3222 014652 022767 000377 001744 CMP #377, TEMP
3223 014660 001401 BEQ .+4
3224 014662 104000 HLT JADCB FAILED
3225 014664 104400 SCOPE
3226 014666 005737 016522 TST #MSAVR6 JPOWER FAIL FLAG
3227 014672 001405 BEQ EAESRT
3228 014674 005037 016522 CLR #MSAVR6
3229 014700 104000 HLT JPOWER FAIL OCCURRED
3230 014702 000137 001034 JMP #NST4 JRESTART PROGRAM
3231 014706 000402 EAESRT: BR .+6 JNOP IF NO EAESRT
3232 014710 000167 000362 JMP ENDEAE
3233 :TEST LEFT SHIFT
3234 014714 104400 SCOPE JTEST OF LOGICAL SHIFT
3235 014716 005077 163426 CLR #MQ JLOAD MQ WITH 0
3236 014722 012777 125252 163422 MOV #125252, #AC JLOAD AC WITH 125252
3237 014730 012777 177760 163430 MOV #-16, #PLSH JLOAD SHIFT COUNT (LSH) WITH -16

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3238 014736 005777 163410 TST @AC ;COMPARE AC WITH 0
3239 014742 001401 BEQ .+4 ;GO TO HLT IF BAD
3240 014744 104000 HLT
3241 014746 022777 125252 163374 CMP #125252,@MQ ;COMPARE MQ WITH 125252
3242 014754 001401 BEQ .+4 ;GO TO HLT IF BAD
3243 014756 104000 HLT
3244 014760 122777 000020 163370 CMPB #20,@SR ;COMPARE SR WITH 2
3245 014766 001401 BEQ .+4 ;SKIP HLT IF GOOD
3246 014770 104000 HLT ;HALT ON ERROR (LEFT SHIFT)
3247
3248 ;TEST RIGHT SHIFT
3249 014772 104400 SCOPE ;TEST OF ARITHMETIC SHIFT
3250 014774 005777 163350 CLR @MQ ;LOAD MQ WITH 0
3251 015000 012777 177777 163344 MOV #-1,@AC ;LOAD AC WITH -1
3252 015006 012777 000020 163354 MOV #16.,@ASH ;LOAD SHIFT COUNT (ASH) WITH 16.
3253 015014 005777 163332 TST @AC ;COMPARE AC WITH 100000
3254 015020 100401 RMI .+4 ;SKIP HLT IF GOOD
3255 015022 104000 HLT ;HALT ON ERROR
3256 015024 005777 163320 TST @MQ ;COMPARE MQ WITH 0
3257 015030 001401 BEQ .+4 ;SKIP HLT IF GOOD
3258 015032 104000 HLT ;HALT ON ERROR
3259 015034 122777 000110 163314 CMPB #110,@SR ;COMPARE SR WITH 10
3260 015042 001401 BEQ .+4 ;SKIP HLT IF GOOD
3261 015044 104000 HLT ;HALT ON ERROR (RIGHT SHIFT)
3262
3263 ;TEST NORMALIZE
3264 015046 104400 SCOPE ;TEST OF NORMALIZE
3265 015050 012777 125252 163272 MOV #125252,@MQ ;LOAD MQ WITH 125252
3266 015056 012777 170000 163266 MOV #170000,@AC ;LOAD AC WITH 170000
3267 015064 005777 163274 CLR @NOR ;START NORMALIZE
3268 015070 022777 100005 163254 CMP #100005,@AC ;COMPARE AC WITH 100005
3269 015076 001401 BEQ .+4 ;SKIP HLT1 IF GOOD
3270 015100 104000 HLT ;HALT ON ERROR
3271 015102 022777 052520 163240 CMP #52520,@MQ ;COMPARE MQ WITH 52520
3272 015110 001401 BEQ .+4 ;SKIP HLT IF GOOD
3273 015112 104000 HLT ;HALT ON ERROR
3274 015114 122777 000003 163232 CMPB #3,@SC ;COMPARE SC WITH 3
3275 015122 001401 BEQ .+4 ;SKIP HLT IF GOOD
3276 015124 104000 HLT ;HALT ON ERROR (NORMALIZE)
3277 ;TEST MULTIPLY
3278 015126 104400 SCOPE ;TEST OF MULTIPLY
3279 015130 012777 125252 163212 MOV #125252,@MQ ;LOAD MQ WITH 125252
3280 015136 012777 040000 163214 MOV #40000,@MUL ;LOAD MUL WITH 40000
3281 015144 022777 165252 163200 CMP #165252,@AC ;COMPARE AC WITH 1652
3282 015152 001401 BEQ .+4 ;SKIP IF GOOD
3283 015154 104000 HLT ;HALT ON ERROR
3284 015156 005777 163156 TST @MQ ;COMPARE MQ WITH 10000
3285 015162 100401 RMI .+4 ;SKIP HLT IF GOOD
3286 015164 104000 HLT ;HALT ON ERROR
3287 015166 122777 0000300 163162 CMPB #300,@SR ;COMPARE SR WITH 300
3288 015174 001401 BEQ .+4 ;SKIP HLT IF GOOD
3289 015176 104000 HLT ;HALT ON ERROR (MULTIPLY)
3290
3291 ;TEST DIVIDE

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3292	015200	104400			SCOPE		;TEST OF DIVIDE
3293	015202	012777	125252	163140	MOV	#125252,@MQ	;LOAD MQ WITH 125252
3294	015210	012777	177777	163134	MOV	#-1,@AC	;LOAD AC WITH -1
3295	015216	012777	000002	163136	MOV	#2,@DIV	;LOAD DIV WITH 2 AND DIVIDE
3296	015224	005777	163122		TST	@AC	;COMPARE AC WITH 0 (QUOTIENT)
3297	015230	001401			REQ	,+4	;SKIP HLT IF GOOD
3298	015232	104000			HLT		;HALT ON ERROR
3299	015234	022777	152525	163106	CMP	#152525,@MQ	;COMPARE MQ WITH 152525
3300	015242	001401			BEQ	,+4	;SKIP HLT IF GOOD
3301	015244	104000			HLT		;DIVIDE ERROR
3302	015246	104400			SCOPE		
3303	015250	012767	177777	001346	MOV	#-1,TEMP	
3304	015256	000261			SEC		
3305	015260	105667	001341		SBCB	TEMP+1	
3306	015264	022767	177377	001332	CMP	#177377,TEMP	
3307	015272	001401			BEQ	,+4	
3308	015274	104000			HLT		

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3309 015276 104400 ENDEAE: SCOPE
3310 015300 022700 052525 CMP #52525,%0
3311 015304 001401 BEQ .+4
3312 015306 104000 HLT
3313 015310 012737 016444 000024 MOV #PFAIL,@#24
3314 015316 012737 000340 000026 MOV #342,@#26
3315 ;SOME OPERATION DESTROYED %0
3316 015324 000421 SKPBEL: BR .+4 ;POWER FAIL VECTOR
3317 015326 000501 BR TRPA
3318 015330 032777 000100 162726 RIT #102,@TTCSR
3319 015336 001006 RNE SBELL
3320 ;BELL ON PASS COMPLETE
3321 015340 012777 000207 000452 RELL: MOV #207,@TDER
3322 015346 105777 000450 TSTB @TCSR
3323 015352 100375 RPL .-4
3324 015354 005237 177570 SBELL: INC @#177570
3325 015360 005227 000000 INC #0
3326 015364 010700 MOV %7,%
3327 015366 042730 017777 RIC #17777,%0
3328 015372 062700 015416 ADD #BEG00,%0
3329 015376 010037 000010 MOV %0,CR10
3330 015402 006701 6701
3331 015404 000240 NOP
3332 015406 012737 000026 015526 MOV #6,CYESRT
3333 015414 000403 BR REGANY
3334 015416 012737 000032 015526 REG20: MOV #2,CYESRT
3335 015424 012737 000012 000010 REGANY: MOV #12,C#10
3336 ;ROUTINE TO CHECK FOR TRACE TRAP TO BE RUN WITH PROGRAM
3337
3338 ;SAVE OLD CONTENTS, SET UP FOR TRACE TRAP
3339 015432 005016 YESRT: CLR (6)
3340 015434 032737 010000 177570 RTI #102,TB,@#SR ;INHIBIT "T" TRAP IF SET
3341 015442 001010 RNE YESRT1
3342 015444 012737 015526 000014 MOV #YESRT,@#14 ;T TRAP VECTOR
3343 015452 005167 000046 COM TRPE
3344 015456 100005 RPL LINKER
3345 015460 012716 000020 MOV #20,(6) ;SET TRACE TRAP
3346 015464 012746 004272 YESTR1: MOV #BEGIN,-(6) ;START OF TEST WITH TRACE ON
3347 015470 000002 YESTR2: RTI
3348 015472 005737 000042 LINKER: TST @#42 ;SHOULD PROGRAM GO TO MONITOR
3349 015476 001406 BEQ LOGICAL ;BR IF NO
3350 015500 012737 015514 000014 MOV #LOGICAL,@#14 ;TO BANK ZERO
3351 015506 000005 RESET ;CLR T BIT IF SET FOR MONITORS
3352 015510 013707 000042 MOV @#42,%7 ;GO TO MONITOR OR ACTII SYSTEM
3353 015514 000763 LOGICAL: BR YESTR1 ;CONTINUE
3354 015516 000240 NOP
3355 015520 000240 NOP
3356 015522 000240 NOP
3357 015524 000000 TRPB: @
3358 015526 000002 YESRT: RTI ;RETURN TO PROGRAM FROM TRAP - CAN BE AN RTT
3359 015530 000000 HALT ;RTI FAILED
3360 015532 000137 004272 TRPA: JMP @#BEGIN ;BEGIN MODIFY BY EXPANSION
3361 015536 000000 PRFLAG: @
3362 ;PRINT ROUTINE BUSY IF NOT ZERO

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3363 ;ENTERED WITH SYSTEM TRAP CALL(HLT)
3364 ;PRINT OUT THE ERROR PC AND STATUS REGISTER
3365 015540 005767 177772 PRINT: TST PRFLAG ;IS ROUTINE BUSY
3366 015544 001401 BEQ .+4
3367 015546 000002 RTI
3368 015550 005267 177762 INC PRFLAG
3369 015554 005227 000000 INC #0
3370 015560 036727 162004 020000 BIT SR,#20000 ;TEST FOR INHIBIT PRINT OUT
3371 015566 001401 BEQ .+4 ;YES EXIT
3372 015570 000473 BR PRINT1 ;NO SET FLAG
3373 015572 012667 000226 MOV (6)*,SAVPC ;ERROR COUNT LOCATION
3374 015576 012667 000224 MOV (6)*,SAVCC ;BRANCH TO PRINT
3375 015602 024646 CMP -(6),-(6) ;INHIBIT, RETURN TO MAIN STREAM
3376 015604 042767 000140 162164 BIC #140,STATUS ;PC OF FAILING ROUTINE
3377 015612 105777 000204 TSTB @TCSR ;CC OF ERROR CONDITION
3378 015616 100375 BPL .-4 ;REPOSITION THE STACK
3379 015620 012777 000215 000172 MOV #215,@TDBR ;WAIT FOR FLAG
3380 015626 105777 000170 TSTB @TCSR ;CR
3381 015632 100375 BPL .-4
3382 015634 012777 000212 000156 MOV #212,@TDBR ;LINE FEED
3383 015642 105777 000154 TSTB @TCSR
3384 015646 100375 BPL .-4
3385 015650 010267 000136 MOV %2,SAVR2 ;SAVE R2
3386 015654 010367 000134 MOV %3,SAVR3 ;SAVE R3
3387 015660 010467 000132 MOV %4,SAVR4 ;SAVE R4
3388 015664 016702 000134 MOV SAVPC,%2
3389 015670 004767 000134 JSR %7,PRTAB ;PRINT OCTAL NUMBER
3390 015674 012777 000240 000116 MOV #240,@TDBR
3391 015702 105777 000114 TSTB @TCSR ;SPACE BETWEEN WORDS
3392 015706 100375 BPL .-4
3393 015710 016702 000112 MOV SAVCC,%2
3394 015714 004767 000110 JSR %7,PRTAB ;PRINT OCTAL NUMBER
3395 015720 012777 000240 000072 MOV #240,@TDBR
3396 015726 105777 000070 TSTB @TCSR
3397 015732 100375 BPL .-4
3398 015734 016702 000444 MOV RETURN,%2 ;WHERE CPU TEST IS AT
3399 015740 004767 000054 JSR %7,PRTAB
3400 015744 016702 000042 MOV SAVR2,%2 ;RESTORE REGISTERS
3401 015750 016703 000040 MOV SAVR3,%3
3402 015754 016704 000036 MOV SAVR4,%4
3403 015760 005767 161684 PRINT1: TST SR ;TEST FOR HALT SWITCH
3404 015764 100001 BPL .+4
3405 015766 000000 HALT ;HALT ON ERROR SET
3406 015770 005067 177542 CLR PRFLAG ;CLEAR FLAG WHEN DONE
3407 015774 032767 000400 161566 BIT #400,SR
3408 016002 001402 BEQ EXPRINT
3409 016024 000167 162500 JMP ESTART ;RESTART ON ERROR
3410 016010 000002 EXPRINT: RTI ;RETURN TO MAIN STREAM
3411 016012 000000 SAVR2: 0
3412 016014 000000 SAVR3: 0
3413 016016 000000 SAVR4: 0
3414 016020 177566 TDBRI 177566 ;DATA
3415 016022 177564 TCSR1 177564 ;STATUS
3416 016024 000000 SAVPC: 0

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3417	016026	000000		SAVCC: 0		
3418		016676		BUFF=FIN	;END OF PROGRAM-SP AREA,	
3419						
3420	016030	005067	000252	PRTAB: CLR	BINCT	
3421	016034	005057	000244	CLR	WGTCR	
3422	016040	012704	316312	MOV	#LIST,%4	
3423	016044	012767	000005	000236	MOV	#5,ASCNT
3424	016052	012767	000027	000220	MOV	#7,SEVEN
3425	016060	012767	000021	000214	MOV	#1,DECML
3426	016066	105777	177730	WAIT1: TSTB	@TCSR	
3427	016072	100375		BPL	WAITS	
3428	016074	005702		TST	%2	
3429	016076	100404		BMI	MINUS	
3430	016100	012777	000260	177712	MOV	#260,@TDRR
3431	016106	000403		RR	STAR	
3432	016110	012777	000261	177702	MINUS: MOV	#261,@TDRR
3433	016116	016703	000156	STAR: MOV	SEVEN,%3	
3434	016122	010267	000150	MOV	%2,TOODLE	
3435	016126	005167	000144	COM	TOODLE	
3436	016132	046703	000140	BIC	TOODLE,%3	
3437	016136	001410		REQ	WRTOC	
3438	016140	066767	000136	000136	MKNUM: ADD	DECML,WGTCR
3439	016146	005287	000134		INC	RINCT
3440	016152	026703	000126		CMP	WGTCR,%3
3441	016156	001370			BNE	MKNUM
3442	016160	062767	000260	000120	WRTOC: ADD	#260,BINCT
3443	016166	016724	000114		MOV	BINCT,(4)+
3444	016172	066767	000122	000102	ADD	SEVEN,DECML
3445	016200	005067	000100		CLR	WGTCR
3446	016204	005067	000076		CLR	BINCT
3447	016210	005367	000074		DEC	ASCNT
3448	016214	001410			BEQ	XLIST
3449	016216	212703	000003		MOV	#3,%3
3450	016222	066767	000032	000050	MOADD: ADD	SEVEN,SEVEN
3451	016230	005303			DEC	%3
3452	016232	001373			RNE	MOADD
3453	016234	000730			BR	STAR
3454	016236	012767	000005	000044	XLIST: MOV	#5,ASCNT
3455	016244	105777	177552		WAIT2: TSTB	@TCSR
3456	016250	100375			BPL	WAIT2
3457	016252	014477	177542		MOV	-(4),@TDDBR
3458	016256	005367	000026		DEC	ASCNT
3459	016262	001401			BEQ	HDFHM
3460	016264	000767			BR	WAIT2
3461	016266	105777	177530		HDFHM: TSTB	@TCSR
3462	016272	100375			BPL	, -4
3463	016274	000207			RTS	%7
3464	016276	000000			TOODLE: 0	
3465	016300	000000			SEVEN: 0	
3466	016302	000000			DECML: 0	
3467	016304	000000			WGTCR: 0	
3468	016306	000000			BINCT: 0	
3469	016310	000000			ASCNT: 0	
3470	016312	000000			LIST: 0	

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3471 016314 000000 0
3472 016316 000000 0
3473 016320 000000 0
3474 016322 000000 0
3475 ;SCOPE LOOP ROUTINE ENTERED BY USER TRAP
3476
3477 ;SCOPE OR/AND ITERATION LOOP FOR EACH TEST 4000 TIMES
3478 016324 032767 040000 161236 SCOPEC: BIT #40000,SR ;TEST SR FOR SCOPE
3479 016332 001012 BNE SCOPEB ;YES SCOPE
3480 016334 032767 004000 161226 BIT #4000,SR ;NO - TEST FOR ITERATION
3481 016342 001011 BNE SCOPEG ;INHIBIT ITERATION
3482 016344 026767 000032 000026 CMP SCOPEF,ICOUNT
3483 016352 001405 BEQ SCOPEG ;EXIT = DONE
3484 016354 005267 000022 INC SCOPEF ;INCREMENT COUNT
3485 016360 016716 000020 SCOPEB: MOV RETURN,%X6 ;REPOSITION THE STACK
3486 016364 000002 RTI ;SCOPE RETURN
3487 016366 005067 000010 SCOPEG: CLR SCOPEF ;CLEAR COUNT
3488 016372 011667 000006 MOV %X6,RETURN ;SAVE SCOPE RETURN POINTER
3489 016376 000002 RTI ;RETURN INLINE-NEXT TEST
3490 016400 004000 ICOUNT: 4000
3491 016402 000000 SCOPEF: 0 ;COUNT LOCATION FOR ITERATION LOOP
3492 016404 004272 RETURN: BEGIN ;ADDRESS OF LAST TEST
3493
3494 ;GROUP OF NESTED SUBROUTINES
3495 016406 000207 SUBR1: RTS X7 ;ONE INSTRUCTION
3496 016410 000277 SUBR2: SCC ;ONE DEEP
3497 016412 000205 SUBR3: RTS X5 ;TWO DEEP
3498 016414 004537 016410 SUBR4: JSR %5,%#SUBR2 ;THREE DEEP
3499 016420 000204 SUBR5: RTS X4 ;FOUR DEEP
3500 016422 004467 177756 SUBR6: JSR %4,SUBR3 ;FIVE DEEP
3501 016426 000203
3502 016430 004367 177756
3503 016434 000202
3504 016436 004267 177756
3505 016442 000207
3506 ;ENTER HERE OR POWER FAIL
3507
3508 016444 010046 PFAIL: MOV X0,-(6) ;SAVE REGISTER OR STACK
3509 016446 010146 MOV X1,-(6) ;WHEN POWERING DOWN
3510 016450 010246 MOV X2,-(6)
3511 016452 010346 MOV X3,-(6)
3512 016454 010446 MOV X4,-(6)
3513 016456 010546 MOV X5,-(6)
3514 016460 016746 161340 MOV 24,-(6)
3515 016464 012737 000002 000006 MOV #RTI,%#6 ;IN CASE OF NO EAE
3516 016472 013746 000352 MOV #AC,-(6)
3517 016476 013746 000350 MOV ##MQ,-(6)
3518 016502 013746 000354 MOV ##SC,-(6)
3519 016506 010667 000010 MOV X6,SAVR6 ;STORE STACK POSITION, POWER FAIL FLAG
3520 016512 012767 016524 161304 MOV #RESTART,24
3521 016520 000000 HALT ;HALT ON POWER DOWN NORMAL
3522 016522 000000 SAVR6: 0 ;STACK IS SAVED HERE
3523 016524 016706 177772 RESTART: MOV SAVR6,X6 ;RESTORE REGISTER OFF STACK
3524 016530 012637 000354 MOV (6)*,%#SC

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3525 016534 012637 000350 MOV (6)*, @#MO ;MO MUST BE LOADED BEFORE AC
3526 016540 012637 000352 MOV (6)*, @#AC
3527 016544 005037 000006 CLR @#6 ;RESTORE TIME OUT
3528 016550 012667 161250 MOV (6)*, 24 ;WHEN POWERING UP
3529 016554 012605 MOV (6)*, %5
3530 016556 012604 MOV (6)*, %4
3531 016560 012603 MOV (6)*, %3
3532 016562 012602 MOV (6)*, %2
3533 016564 012601 MOV (6)*, %1
3534 016566 012600 MOV (6)*, %0
3535 016570 000002 RTI ;RETURN TO MAIN LINE
3536 016572 125252 B: 125252
3537 ;FIXED VALUES FOR USE IN TEST R
3538 016574 016572 052525 ;ADDRESS OF R
3539 016576 052525
3540
3541 016602 .=B+10
3542 016602 177777 A: -1
3543 016604 016606 A+4
3544
3545 016606 .=A+4
3546 016606 125252 125252
3547 016610 016612 A+10
3548 016612 052525 052525 ;ADDRESS OF A+10
3549 ;FOR STORAGE
3550 016614 000000 C: 0
3551 016616 016614 C ;ADDRESS OF C
3552
3553 016624 .=C+10
3554 016624 000000 TEMP: 0
3555 016626 016624 TEMP ;ADDRESS OF TEMP
3556
3557 016632 .=TEMP+6
3558 016632 016634 TEMP+10 ;ADDRESS OF TEMP+10 OR "D"
3559 016634 000000 D: 0
3560 016676 .=..+40
3561 016676 000000 FIN: 0 ;BUFFER FOR SP
3562 016700 000207 USER: RTS %7 ;OVERLAY USER ROUTINE HERE IF 4K, USE BANK1 IF >4K
3563 ;PDP-11 MEMORY DETERMINATION AND SETUP
3564 ;USE WITH VARIABLE CORE QUANTITY SYSTEMS
3565 016702 .=FIN + 4 ;APPLICABLE TO SYSTEM TEST 21
3566 016702 012767 004272 176624 DET1: MOV #BEGIN, TRPA+2
3567 016710 012767 000401 176406 MOV #401, SKPREL ;BR ,+4
3568 016716 023727 000042 016702 CMP @#42, #DET1 ;CHECK FOR DDP1
3569 016724 101401 BLOS .+4
3570 016726 000207 RTS %7 ;NO CORE EXPANSION WITH DDP1
3571 016730 032767 001000 160632 BIT #1000, SR ;CHECK VARIABLE CORE SWITCH
3572 016736 001401 REQ DET4 ;USE VARIABLE CORE ROUTINE
3573 016740 000207 RTS %7 ;4K ONLY
3574 016742 012767 017010 161034 DET4: MOV #DET2, 4 ;TRAP VECTOR SETUP
3575 016750 012767 000340 161030 MOV #340, 6 ;TRAP STATUS SETUP
3576 016756 005537 037770 EIGHT: ADC @#37770 ;CHECK FOR 8K
3577 016762 005537 057770 TWELVE: ADC @#57770 ;CHECK FOR 12K
3578 016766 005537 077770 SIXTEEN: ADC @#077770 ;CHECK FOR 16K

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3579	016772	005537	117770	TWENTY:	ADC	@#117770	;CHECK FOR 20K
3580	016776	005537	137770	TWOFOR:	ADC	@#137770	;CHECK FOR 24K
3581	017002	005537	157770	TWOEIG:	ADC	@#157770	;CHECK FOR 28K
3582	017006	000430		BR		STRT28	
3583	017010	012602		DET21	MOV	(6)+,%2	;RETRIEVE TRAP PC
3584	017012	005726			TST	(6)*	;DISCARD TRAP STATUS WORD
3585	017014	022702	016762		CMP	#EIGHT+4,%2	
3586	017020	001542			BEQ	DET3	;4K
3587	017022	022702	016766		CMP	#TWELVE+4,%2	
3588	017026	001437			BEQ	STRT8	;8K
3589	017030	022702	016772		CMP	#SIXTEEN+4,%2	
3590	017034	001431			BEQ	STRT12	;12K
3591	017036	022702	016776		CMP	#TWENTY+4,%2	
3592	017042	001423			BEQ	STRT16	;16K
3593	017044	022702	017022		CMP	#TWOFOR+4,%2	
3594	017050	001415			REQ	STRT20	;20K
3595	017052	000411			BR	STRT24	;24K
3596	017054	005000		MOVE1:	CLR	%0	;SET UP MAIN CORE CURRENT
3597	017056	012021			MOV	(0)+(1)+	;MOVE WORD
3598	017060	020027	016700		CMP	%0,#FIN+2	;MOVE COMPLETE?
3599	017064	001374			BNE	-6	;MOVE ANOTHER WORD
3600	017066	000207			RTS	%7	;MOVE COMPLETE
3601	017070	004767	000040	STRT28:	JSR	%7,XFER28	;START 28K TRANSFER
3602	017074	000450			BR	MOD24	;START 24K MODIFY
3603	017076	004767	000042	STRT24:	JSR	%7,XFER24	;START 24K TRANSFER
3604	017102	000453			BR	MOD20	;START 20K MODIFY
3605	017104	004767	000044	STRT20:	JSR	%7,XFER20	;START 20K TRANSFER
3606	017110	000456			BR	MOD16	;START 16K MODIFY
3607	017112	004767	000046	STRT16:	JSR	%7,XFER16	;START 16K TRANSFER
3608	017116	000461			BR	MOD12	;START 12K MODIFY
3609	017120	004767	000050	STRT12:	JSR	%7,XFER12	;START 12K TRANSFER
3610	017124	000464			BR	MOD8	;START 8K MODIFY
3611	017126	004767	000052	STRT8:	JSR	%7,XFER8	;START 8K TRANSFER
3612	017132	000467			BR	MOD4	;START 4K MODIFY
3613	017134	012701	140000	XFER28:	MOV	#140000,%1	;SET UP MOVE START LOCATION
3614	017140	004767	177710		JSR	%7,MOVE	;GO TO MOVE SUBROUTINE
3615	017144	012701	120000	XFER24:	MOV	#120000,%1	
3616	017150	004767	177720		JSR	%7,MOVE	
3617	017154	012701	100000	XFER20:	MOV	#100000,%1	
3618	017160	004767	177670		JSR	%7,MOVE	
3619	017164	012701	060000	XFER16:	MOV	#60000,%1	
3620	017170	004767	177650		JSR	%7,MOVE	
3621	017174	012701	040000	XFER12:	MOV	#40000,%1	
3622	017200	004767	177650		JSR	%7,MOVE	
3623	017204	012701	020000	XFER8:	MOV	#20000,%1	
3624	017210	004767	177640		JSR	%7,MOVE	
3625	017214	000207		RTS		%7	;RETURN FROM TRANSFERS
3626	017216	012767	144300	116310	MOD24:	MOV	#BEGIN+140006,TRPA+120002
3627	017224	012767	000240	116072	MOV	#NOP,SKPBL+120000	
3628	017232	012767	124300	076274	MOD20:	MOV	#BEGIN+120006,TRPA+100002
3629	017240	012767	000240	076056	MOV	#NOP,SKPBL+100000	
3630	017246	012767	104300	056260	MOD16:	MOV	#BEGIN+100006,TRPA+60002
3631	017254	012767	000240	056042	MOV	#NOP,SKPBL+60000	
3632	017262	012767	064300	036244	MOD12:	MOV	#BEGIN+60006,TRPA+40002

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3633 017270 012767 000240 036026      MOV    #NOP,SKPREL+40000
3634 017276 012767 044300 016230  MOD8:  MOV    #BEGIN+40006,TRPA+20002
3635 017304 012767 000240 016012      MOV    #NOP,SKPREL+20000
3636 017312 012767 024300 176214  MOD4:  MOV    #BEGIN+20006,TRPA+2
3637 017320 012767 000240 175776      MOV    #NOP,SKPREL
3638 017326 000207                 DE13:  RTS    %7          ;RETURN FROM MODIFY
3639 000001                 .END
```

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A	016602	AC	000352	ADSUB	014130	ARIEND	014172
ARITST	014104	ASCNT	016310	ASH	000370	B	016572
BEGANY	015424	BEGIN	004272	BEG20	015416	BELL	015340
BINCT	016306	BR	= 000002	BUFF	= 016676	C	016614
CC	= 177776	CLINST	002132	CMP1	013430	CMP2	013452
COMPAR	013424	CURPAT	002126	D	016634	DATA1	001436
DATA2	001464	DATA3	001540	DATA4	001634	DECML	016302
DELAY	001640	DET1	016702	DET2	017010	DET3	017326
DET4	016742	DIV	000362	DO	= 000001	EAESRT	014706
EIGHT	016756	ENDEAE	015276	ESTART	000510	EXPRIN	016010
F	= 000000	FENDZ	002534	FEND1	002556	FIN	016676
HDFHM	016266	HLT	= 104000	HPCSP	000274	HPDBR	000276
HPOUT	001542	HPOUTR	001560	HPOUT1	001550	HPOUT2	001624
HRCSR	000270	HRDBR	000272	HSRINR	001466	HSRINI	001524
HSRIN2	001532	ICOUNT	016400	IE	= 000100	INTCNT	001636
IRC	002352	IRF	002450	IRK	002164	IRP	002266
LINKER	015472	LIST	016312	LKCSR	000300	LK1	001642
LK2	001662	LK3	001664	LK4	001702	LLIMIT	002522
LOGICA	015514	LPCSR	000302	LPDBR	000304	LPINTR	002006
LP1	001762	LP2	001770	LP3	002450	LP4	002062
LP5	002116	LP6	002016	LSH	000366	MAINLI	001344
MINUS	016110	MKNUM	016140	MOADD	016222	MOD12	017262
MOD16	017246	MOD20	017232	MOD24	017216	MOD4	017312
MOD8	017276	MOVE	017054	MQ	000350	MUL	000360
N	= 000001	NOEAE	000472	NOP	= 000240	NOR	000364
NUMA	014170	PFAI	- 016444	PRFLAG	015536	PRINT	015540
PRINT1	015760	PRTAB	016030	R	= 004000	RB	= 000002
RCBAR	000326	RCCSR	000330	RCCSRH	000332	RCDAR	000322
RCFUNC	002410	RCSTAR	002320	RCWC	000324	RCWORD	= 176040
RC2	002326	RD	= 000004	REF	= 013616	REFF	013616
REG1	001362	RENDZ	002722	REND1	002752	RESTAR	016524
RETURN	016404	RFCAR	000314	RFCSR	000316	RFCSRH	000320
RFDAE	000306	RFDAR	000310	RFFUNC	002520	RFSTAR	002412
RFWC	000312	RFWORD	= 176040	RF1	002424	RKBAR	000342
RKCSR	000344	RKCSRH	000346	RKDAE	000336	RKDAH	000334
RKFUNC	002226	RKSTAR	002134	RKWC	000340	RKWORD	= 176002
RK1	002140	ROTALL	013506	ROTBE	013656	ROTBO	013766
ROTEM1	014070	RPBAR	000424	RPCA	000410	RPCSR	000426
RPCSRH	000430	RPDAE	000414	RPDAH	000412	RPDAR	000420
RPDSR	000416	RPFUNC	000432	RPSTAR	002230	RPWC	000422
RPWORD	= 176000	RP1	002242	RSR	=%000002	R100	=%000000
R101	=%000001	SAVCS	016026	SAVPC	016024	SAVR2	016012
SAVR3	016014	SAVR4	016016	SAVR6	016522	SABELL	015354
SC	000354	SCOPE	= 104400	SCOPEB	016360	SCOPEC	016324
SCOPEF	016402	SCOPEG	016366	SEVEN	016300	SKPBEL	015324
SOLPAT	002130	SR	= 177570	SRE	000356	STAR	016116
START	000502	START2	000566	STATUS	= 177776	STR12	017120
STR16	017112	STRT20	017104	STRT24	017076	STRT28	017070
STRT8	017126	ST1	000756	ST2	000770	ST3	001010
ST4	001034	ST5	001052	ST5A	001122	ST6	001200
ST7	001226	ST8	001310	SUBR1	016406	SUBR2	016410
SUBR3	016414	SUBR4	016422	SUBR5	016430	SUBR6	016436
SWABA	014566	SXTEEN	016766	TC	= 177340	TCBA	000404
TCBLK	002530	TCCM	000372	TCDT	000376	TCEXPE	002532

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TCFIRS	002524	TCF1	002606	TCF1A	002600	TCF2	002634
TCF3	002650	TCF4	002712	TCIV	002406	TCLAST	002526
TCOM	014204	TCOM2	014252	TCOM3	014320	TCRBK	003172
TCRBUF	003256	TCRB1	003230	TCR1	003050	TCR1A	003102
TCR2	003106	TCR3	003122	TCR4	003164	TCGR	016022
TCST	000374	TCWB1	002770	TCWBUF	003256	TCWB1	003022
TCWC	000402	TC1	000434	TC2	002446	TDBR	016022
TDSR	= 016022	TEMP	016624	TEST	013620	TIME	001762
TJSR1	013030	TJSR2	013032	TJSR3	013044	TOODLE	016276
TRCSR	000260	TRDR	000262	TRPA	015932	TRPB	015524
TSCOMB	014362	TSROT	013464	TSROT2	013530	TSRT2A	013622
TSTAR1	014072	TTCSR	000264	TTDBR	002266	TTYINR	001364
TTYIN1	001422	TTYIV2	001430	TTYIN3	001414	TTYIN4	001420
TWELVE	016762	TWENTY	016772	TWOEIG	017002	TWOFOR	016776
TYOUTR	001440	TYOUT1	001454	USER	016700	WAIT1	016066
WAIT2	016244	WAIT3	014432	WAIT4	014502	WAIT5	014454
WD	= 000014	WGCTC	016304	WRTOP	016160	XFENDZ	002720
XFER12	017174	XFER16	017164	XFER20	017154	XFER24	017144
XFER28	017134	XFERB	017204	XLIST	016236	XX	= 000022
YESRT	015526	YESRT	015432	YESRT1	015464	YESRT2	015478
	* 017330						

ERRORS DETECTED: 0

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T17QE4

*T17QE4,T17QE4/SOL-T1/QE4
RUN-TIME: 15 30 0 SECONDS
CORE USED: 9K